ADVANCED PLASMA-ETCHING PROCESSES FOR DIELECTRIC MATERIALS IN VLSI TECHNOLOGY

By

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ADVANCED PLASMA-ETCHING PROCESSES FOR DIELECTRIC MATERIALS IN VLSI TECHNOLOGY

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Manufacturable plasma etching processes for dielectric materials have played an important role in the Integrated Circuits (IC) industry in recent decades. Dielectric materials such as SiO_2 and SiN are widely used to electrically isolate the active device regions (like the gate, source and drain from the first level of metallic interconnects) and to isolate different metallic interconnect levels from each other. However, development of new state-of-the-art etching processes is urgently needed for higher aspect ratio (oxide depth/hole diameter—6:1) in Very Large Scale Integrated (VLSI) circuits technology. The smaller features can provide greater packing density of devices on a single chip and greater number of chips on a single wafer.

This dissertation focuses on understanding and optimizing of several key aspects of etching processes for dielectric materials. The challenges are how to get higher selectivity of oxide/Si for contact and oxide/TiN for vias; tight Critical Dimension (CD) control; wide process margin (enough over-etch); uniformity and repeatability. By

exploring all of the parameters for the plasma etch process, the key variables are found and studied extensively. The parameters investigated here are Power, Pressure, Gas ratio, and Temperature. In particular, the novel gases such as C_4F_8, C_5F_8, and C_4F_6 were studied in order to meet the requirements of the design rules. We also studied CF_4 that is used frequently for dielectric material etching in the industry. Advanced etch equipment was used for the above applications: the medium-density plasma tools (like Magnet-Enhanced Reactive Ion Etching (MERIE) tool) and the high-density plasma tools.

By applying the Design of Experiments (DOE) method, we found the key factors needed to predict the trend of the etch process (such as how to increase the etch rates, selectivity, etc.; and how to control the stability of the etch process). We used JMP software to analyze the DOE data.

The characterization of the etch processes included measurement of the etch rates, etch profiles, etch depth, top-down images, selectivity and etch margin. The cross-section images were taken on the Hitachi S-4500 Scanning Electron Microscope (SEM, Tokyo, Japan) tool.

CHAPTER 1
INTRODUCTION

1.1 Processes for Manufacturing Integrated Circuits (IC)

In 1959, Jack Kilby formed a complete circuit on a single piece of the semiconducting material germanium. His invention combined several transistors, diodes and capacitors and used the natural resistance of the germanium chip as a circuit resistor. This invention was the Integrated Circuit (IC), the first successful integration of a complete circuit in and on the same piece of a semiconducting substrate. The techniques used not only met the needs of that era, but also contained seeds for all of the miniaturization and cost-effective manufacturing that still drives modern industry.[1] There are two common trackers of IC development: device component size and the number of components in an IC. Device component size is also called the feature size, and is usually expressed by the length of the gate and in microns. The number of components in an IC is also called the circuit density. It is characterized by the integration level in the design. The integration level ranges from Small Scale Integration (SSI) to Very Large Scale Integration (VLSI) and to Ultra Large Scale Integration (ULSI).

The product trends in IC industry are as follows:

- Decreasing the feature size. The circuit density can be increased dramatically by reductions in the feature size of the individual components because the components are crowded closer together at this point. Reduction of the feature size has two benefits: one is higher circuit speed (because of less distance to travel); and the other is that individual devices occupy less space and require less power to operate.
- Increasing chip and wafer size. Placing square or rectangular chips on a round wafer leaves unavailable areas around the edge. The desire to offset the loss of usable

silicon has driven the industry to larger wafers. Some companies are currently developing the process for 300 mm (diameter) wafers.

- Reducing the defect density. It is very critical to reduce the defect density when the feature size is decreased significantly, because the small defect becomes a killer and can render the component inoperable. Therefore, contamination control is highly demanded in IC manufacture.

- Increasing the interconnection levels. The component density increase has led to a "wiring" problem. The reason is that the increased component density and close packing rob the surface space needed on the surface to connect the components. The solution is multiple levels of "wiring" stacked above the surface components in layers of insulators and conducting layers.

- Reducing the chip cost. The cost of the chips is the most significant effect of the process and product improvements in IC fabrication. The high performance devices need to be delivered to the customers at lower cost. The strategies to reduce the chip cost include maximizing equipment cost of ownership, automation, cost control, computer-automated manufacturing, computer-integrated manufacturing, and statistical process control.

Modern chip structures have multiple layers and pockets of dopants (numbers of layers added to the surface) including multiple layers of conductors interspersed with dielectrics. Achieving these complicated structures requires many processes. Each process in turn requires a number of steps and substeps. There are four basic operations in an infinite number of sequences and variations to produce specific microchips. They are deposition, doping, patterning and etching, and heat treatments.

- Deposition. This is used to deposit thin films on the wafer surface. These layers could be insulators, semiconductors, or conductors. The common deposition techniques are Chemical Vapor Deposition (CVD), Plasma-Enhanced Chemical Vapor Deposition (PECVD), evaporation, and sputtering.

- Doping. This puts specific amounts of dopants in the wafer surface through openings in the surface layers. The two major techniques are thermal diffusion and ion implantation. Thermal diffusion is a chemical process that occurs when the wafer is heated to the vicinity of 1000 °C, and is exposed to vapors of the proper dopants. Ion implantation is a physical process. Wafers are loaded in one end of an implanter and dopant sources are in the other end. At the source end, the dopant atoms are ionized and accelerated to a high speed, and the beam swept across the wafer surface. The purpose of the doping is to create either N-type (rich in electrons) or P-type (rich in holes). These N-P junctions are required for operation of the transistors, diodes, capacitors, and resistors of the circuit.

- Patterning and etching. The goal of the patterning and etching operations is to create the desired shapes in the exact dimensions required by the circuit design, and to place them in their proper location on the wafer surface and in relation to the other parts of the transistors, diodes, capacitors, resistors and metal conduction system.

- Heat treatments. The wafer is simply heated and cooled to achieve specific results. No additional material is added or removed from the wafer during the heat treatments. A very important heat treatment takes place after ion implantation. This process is called annealing. It can repair the disruption of the wafer crystal structure caused by the implantation of the dopant atoms.

Figure 1 shows the manufacturing processes of ICs from the circuit design to the final IC products. Figure 2 shows more details of CMOS fabrication steps in the industry.

Particularly, the importance of constant testing needs to be emphasized throughout the process. The wafer fabrication process requires a high degree of precision in process control, equipment operation, and material manufacture. One mistake can render the wafer completely useless. Therefore, a variety of tests and measurements are made to determine both wafer and process quality. The tests take place on in-process wafers, test die and production die, and the finished circuit.

1.2 Challenges of Etching Processes for Dielectric Materials

It is very important to develop the stable plasma etching process for dielectric materials in the fabrication of the Complementary Metal Oxide Semiconductor (CMOS) circuits because of their isolation function. The dielectric materials include Silicon Dioxide (SiO_2) and Silicon Nitride (SiN).

There are two categories within the oxide etch process: contact etching and via etching. As shown in Figure 3, both contact and via are filled by Tungsten (W). The contact was created in the oxide between the active regions and the first metallic

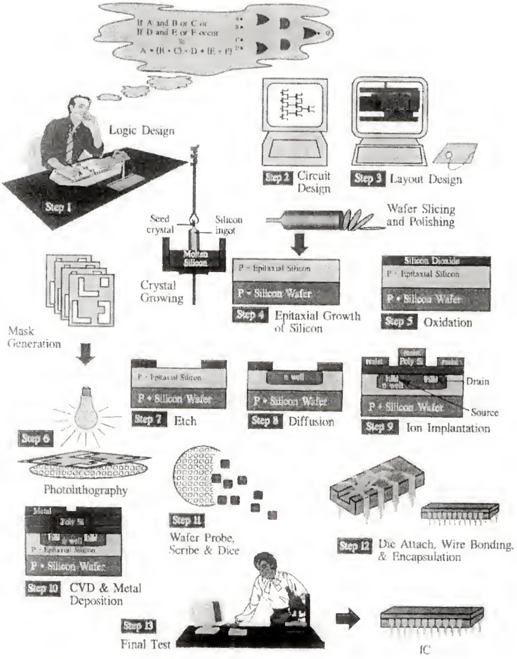


Figure 1. Processes for manufacturing integrated circuits

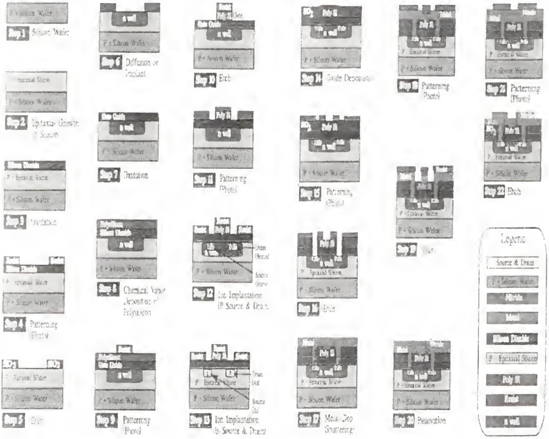

Step 1 Silicon Wafer
Step 6 Diffusion or Implant
Step 10 Etch
Step 14 Oxide Deposition
Step 18 Patterning (Photo)
Step 21 Patterning (Photo)
Step 2 Epitaxial Growth of Silicon
Step 7 Oxidation
Step 11 Patterning (Photo)
Step 15 Patterning (Photo)
Step 22 Etch
Step 3 Oxidation
Step 8 Chemical Vapor Deposition of Polysilicon
Step 12 Ion Implantation (P Source & Drain)
Step 16 Etch
Step 19
Step 4 Patterning (Photo)
Step 5
Step 9 Patterning (Photo)
Step 13 Ion Implantation (n Source & Drain)
Step 17 Metal Dep Sputtering
Step 20 Passivation
Silicon Wafer
n well
Poly Si
Gate Oxide
Silicon Dioxide
Epitaxial Silicon
SiO2
Drain
Source
Legend
Source & Drain
P - Silicon Wafer
Nitride
Metal
Silicon Dioxide
P Epitaxial Silicon
Poly Si
Resist
n well

Figure 2. Complementary Metal-Oxide Semiconductor (CMOS) fabrication process steps

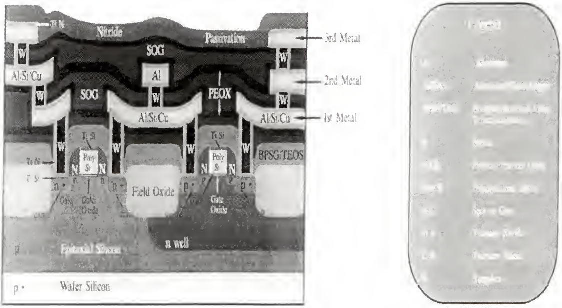


Figure 3. Film stacks of three metal layers on CMOS device

interconnect level and was also called window-1 etch. For Embedded Static Random Access Memory (ESRAM) Circuits,[1] there is another type of contact etching – Self-aligned Contact (SAC) etching that is more complicated than the regular contact etch process. Both the etch processes for SiO_2 and SiN (Nitride etch process) need to be developed at the same time. All of the processes in VLSI fabrication before Metal One are called Front End of Line (FEOL); Back End of Line (BEOL) defines the processes after Metal One. Vias are the holes created between metallic interconnect levels. They are called window-2, 3, 4, 5 and depend on the different interconnect levels. Holes that are etched in the oxide are filled by Tungsten (W) or Copper (Cu) to create electrical contacts to the devices and in between levels of wiring. In order to lower the seam for the Tungsten (W) plugs deposited, the tapered via etch process (round corner) is required for the analog circuits.

In regular contact etching, the process must stop on one of the following materials: crystalline Silicon (c-Si), and Tungsten Silicon (WSi_x) or doped poly-Si. In SAC etching, the process has to stop on the SiN layer first, and then apply the SiN breakthrough process to stop on either poly-Si or crystalline Si. In via etching, the process must stop on a Titanium Nitride (TiN) layer which is the top layer of metal interconnect stack. All of the above requirements ask for higher selectivity of oxide/Si, oxide/ TiN and oxide/ SiN.

Fluorinated chemistries such as CF_4, C_4F_8, C_5F_8, C_4F_6 are used for contact and via etching as they allow fast etch rates. Usually they are combined with hydrocarbon chemistries (CH_2F_2 or CHF_3) that enhance polymer deposition during etching and improve the selectivity. Chemically nonreactive noble gases are also added sometimes to change the sputtering component of the etching. Because Fluorine (F) atoms etch both Photo-Resist and oxide, while CF_x species etch primarily oxide, the fluorine-to-carbon ratio must be carefully controlled to maintain high selectivity with reasonable oxide etch rates.[2-7]

The tight Critical Dimension (CD) control in dielectric etching is very important in VLSI technology because more vertical profiles allow for closer packing density of the underlying devices. A taper angle of 88 to 89° is often desirable for easier filling by the metallic plugs such as W or Cu. Normally the diameter of the contact holes is smaller than the vias based on the design rules. Control of CD is more difficult for higher aspect ratio features because the balance of etching and deposition processes can also vary with the depth. Usually we use either top-down CD SEM (Hitachi-9400, Tokyo, Japan) to measure the inner/outer diameter inline without breaking the wafers or SEM (Hitachi S-4500, Tokyo, Japan) to have the cross-section done upon cleaving the wafer. A major goal is to have deeper etching and maintain the CD from top to bottom of the contact and vias for the process development engineers.

For fabrication of the deep submicron features, single-wafer etchers are more popular than batch tools in the industry. Repeatability and uniformity from wafer to wafer and lot to lot are improved by using these single-wafer etch tools. Figure 4 shows the configuration of Magnetic-Enhanced Reactive Ion Etching (MERIE) tool. A single RF power source is applied to the lower electrode and the upper electrode is grounded. The magnetron principle from sputter deposition is adapted to make the primary electron excitation process in plasma etchers more efficient at middle gas pressures. As a result, both higher reactant species production and greater ion bombardment rates of the surfaces

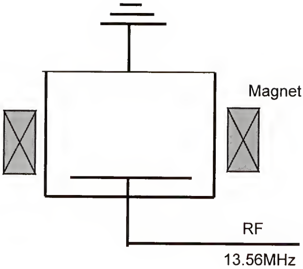


Figure 4. Configuration of the medium-density plasma etcher

being etched can be achieved at lower pressures, namely 20 to 200 mTorr, while still maintaining the high etch rates necessary for adequate throughputs in single wafer etchers.[7] The slowly rotating magnetic field is around 120 Gauss. This type of etch tool is also called a medium-density plasma etcher (ion density – 10^{11} ions/cm^3) since the plasma density is lower than in high-density plasma sources and higher than in the plasmas of conventional parallel-plate reactors. This medium-density plasma etcher can provide better uniform plasma compared with the conventional MERIE because of the gradient magnetron. Figure 5 shows the mechanism of the conventional MERIE. The Lorentz relation combines the effect of electric and magnetic fields. Electrons migrate to the left with positive charges also migrating to the left but at a slower rate. Consequently, the ion density and plasma density are higher. The result of this phenomenon is a higher potential difference from the left side to the right side of the wafer with current flowing in a counterclockwise motion, resulting in a delta Vdc. This potential difference results in charge build-up in the device and ultimately gate oxide damage. Figure 6 shows the mechanism of the gradient MERIE that is also called Dipole Ring Magnetron (DRM). The electrons drift from East to West, parallel to electrode. High plasma density is achieved by the magnetic field and the electrons' collision probability with ions is increased. Figure 7 shows the comparison of the plasma density between the conventional and gradient MERIE. The gradient MERIE can provide better uniform plasma. Figure 8 shows the chamber configuration of a high-density plasma etcher (ion density: 10^{12} ions/cm^3). It has advantages such as highly anisotropic etching due to the low pressure, high etch rates due to the high ion density, and good selectivity.[8] It is very useful for filling high-aspect ratio trenches and holes found in deep submicron circuit

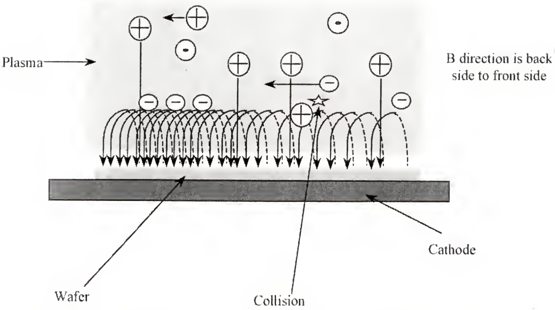


Figure 5. Mechanism of the conventional Magnetic-Enhanced Reactive Ion Etching (MERIE)

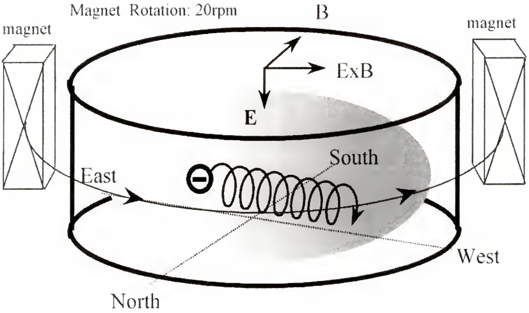
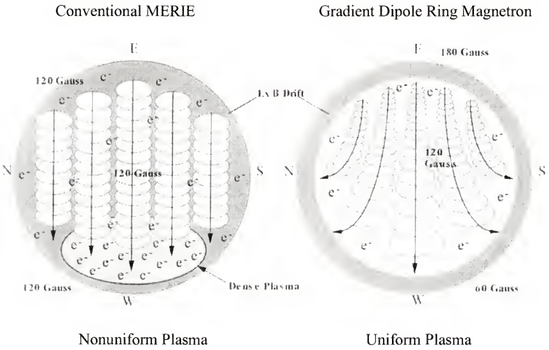


Figure 6. Mechanism of the gradient MERIE



Conventional MERIE

Gradient Dipole Ring Magnetron

Nonuniform Plasma

Uniform Plasma

Figure 7. Comparison of the plasma density between the conventional MERIE and gradient MERIE

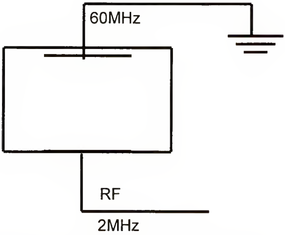


Figure 8. Configuration of the high-density plasma etcher

topographies without the build-up of overhangs on the upper corners of the feature that eventually causes void formation.[7]

1.3 Dissertation Goal and Scope

This dissertation investigates the challenges for the etching processes of dielectric materials in VLSI technology. Emphasis focuses on achieving higher selectivity of SiO_2 over TiN and SiO_2 over SiN, controlling smaller CD variation before and after the etching process, improving the process margin for higher volume manufacturing, and getting better uniformity from wafer to wafer and from lot to lot. All of the work is directed towards optimizing the etching processes for the dielectric materials: SiO_2 and SiN by exploring the etching parameters. Particularly, the different etching processes are attempted based on the different requirements from the design rules and integration viewpoints. Finally, the optimized etching processes are delivered to the manufacturing lines.

Chapter 1 introduces the processes in the IC manufacturing industry and the challenges for developing the etching process for dielectric materials.

Chapter 2 describes two different etching methods applied in the semiconductor fabrication field and the physical mechanisms of plasma etching process. The etching equipment is also reviewed based on the various applications.

Chapter 3 starts with the function of contact in IC fabrication. The contact etching process is developed and finalized with a high aspect ratio up to 5:1. The medium-density plasma etcher is able to manufacture for 0.18 μm and below technologies.

Chapter 4 presents the requirements for via etch process. The main etch parameters such as pressure, power and gas flows are studied extensively in order to meet longer over etch, higher selectivity of SiO_2 over TiN. The DOE is executed carefully to find the key parameters for the via etch process. By analyzing the DOE results, we can predict the process trend if any etching parameters vary during the process. It is helpful to check the process margin and repeatability of the process. The Plasma-Induced Damage (PID) issue is addressed among different etchers and different etch processes. Lower power causes less plasma damage according to the electrical results of several split lots.

Chapter 5 discusses the special via etching process – the tapered via process for the particular application in Analog circuits. The Ex-situ process for 0.25 μm technology is implemented in the production lines successfully. It provides lower contact resistance and much higher yield than the nontapered via etching process. The Ex-situ etching process is evaluated first for 0.18 μm and below technologies due to the timeframe of manufacturing. Tapered via with the straight profile on the bottom of vias has been obtained by using the medium-density plasma etching tool. However, there are two drawbacks for this process: one extra etch step after Photo-Resist (PR) strip decreases the throughput and the thicker oxide layer deposition requires more over-etch margin. Therefore, In-situ processes for the smaller feature size technologies needs to be developed in order to reduce the cycle time and cost of ownership.

Chapter 6 presents another special contact etching process – Self-aligned Contact (SAC) etching process used in the Embedded Statistics Random Access Memory (ESRAM) circuits. It is more challenging than the regular contact etching process because a higher selectivity of SiO_2 over SiN (up to 20:1) is required. The novel gases such as C_5F_8 and C_4F_6 are studied among different types of etching tools. Finally, the "backup process" is developed and implemented in the manufacturing lines after the yield data is collected on several split lots.

Chapter 7 gives the conclusions of the work and suggests future research in VLSI technology.

CHAPTER 2
ETCHING PROCESSING: THEORY AND BACKGROUND INFORMATION

2.1 Etching Methods

"Etching" is used to describe any technique by which material can be uniformly removed from a wafer, or locally removed as in the transfer of patterns during fabrication of a microcircuit.[9, 10] There are two different etching methods that use two quite different media: liquid chemicals (wet etching) and reactive gas plasmas (dry etching). The basic mechanism of wet chemical etches of semiconductors is the formation of an oxide, or oxides on the surface, and the subsequent dissolution of the oxidized products by either acids or bases.[11-20] This etching method has many advantages for device fabrication such as simplicity, high selectivity, high throughput and low cost. However, the isotropic nature of wet chemical etching is not able to meet the requirements developed for increasing circuit density and narrower line-width in the manufacture of VLSI devices. It became necessary to have dry etching to replace wet chemical etching. Dry etching is also called plasma etching since most dry etching processes use a low pressure gas in the form of a plasma to provide etchants. The most significant advantage of dry over wet etching is that it provides higher resolution potential by overcoming the problem of isotropy. Other benefits are the reduced chemical hazard and waste treatment problems, and the ease of process automation and tool clustering that is very important for manufacturing.[8] Therefore, dry etching has been predominant in VLSI fabrication for the past several decades.

2.2 Mechanisms of the Dry Etching Process

A plasma is a gas that contains equal numbers of positive and negative charges, neutral atoms, radicals or molecules, in addition to photons emitted from excited species. Radicals are molecule fragments with unsaturated bonds. Positive charge carriers are mostly ionized atoms, radicals, or molecules created by impact with energetic electrons. Most negative charges are free electrons. In the presence of atoms with high electron affinity, negatively charged ions can be created when these capture plasma electrons. Neutral atoms, radicals and molecules can be in the ground or excited state. Photons are emitted when excited species lose energy via spontaneous transitions to lower energy states. This latter process is the basis for the "glow" of the discharge.[18, 21, 22]

The plasma can be created by applying an electric field of sufficient magnitude to a gas. The process can be initiated by an incident electron which gains kinetic energy from the applied electric field. The probability for the electron to collide with and transfer energy to a gas atom or molecule depends on the electron energy, the gas pressure, and the dimensions of the plasma chamber. When a collision occurs, it results in ionization, excitation, or fragmentation of gas molecules. An ionizing collision generates an electron-ion pair. The two new charged particles are accelerated in the electric field and can in turn collide with and ionize other gas particles. As this process continues, the gas breaks down and the plasma is created. The charged particles can be neutralized by recombination within the plasma or at the chamber walls. For a plasma to be sustained, however, the rate of ionization of gas atoms or molecules must be equal to the rate of electron and ion recombination.[18]

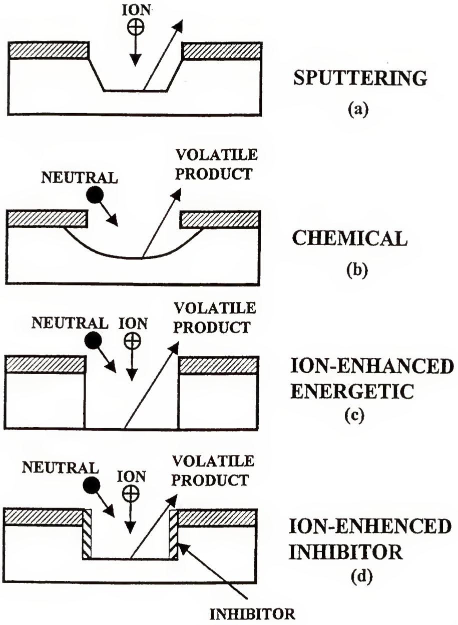


Figure 9. Four basic mechanisms of dry etching

The four basic categories for the mechanisms of the dry etching process are shown in Figure 9:

- Sputtering. The interaction is purely physical and momentum transfer is involved. Sputtering is dominated by the acceleration of energetic ions formed in the plasma to the substrate surface at relatively high energies, typically > 200 eV. Due to the transfer of energy and momentum to the substrate, material is ejected from the surface. The advantage of this sputtering mechanism is anisotropic profiles. However it can result in rough surface morphology, trenching, poor selectivity thus minimizing device performance and causing damage to the devices. The etch rates are very slow that increases the cycle time in the industry. The etch rate, R, is directly proportional to the sputter yield (the number of sputtered atoms or molecules per incident ion), given by

  $$R = 6.22 sjW/\rho \quad (\mathrm{nm/min})$$

  Where s is the sputter yield, j is the ion flux ($\mathrm{mA/cm^2}$), W is the molecular weight of the etched material (g/mol), and ρ is the density of the material to be etched ($\mathrm{g/cm^3}$).[18]

- Chemical. The gas mixture is chosen to produce reactive species by molecular dissociation into radicals and excitation of neutrals in the plasma. Chemically dominated etch mechanisms rely on the formation of reactive species in the plasma that adsorb to the surface, form volatile etch products, and then desorb from the surface. The key requirement for successful chemical etching is the volatility (or ability to evaporate) etch products. Good etch rates and selectivity can be obtained, and the plasma-induced damage is minimized. But it is usually non-directional (isotropy) and cannot maintain the smaller CD needed in VLSI manufacturing processes because of the absence of physical enhancement.

- Ion-enhanced energetic mechanism. There is little surface reaction with neutral radicals. Impinging ions damage the substrate material by virtue of their impact energy, and thereby render the solid substrate more reactive toward incident neutral radicals. This process offers highly anisotropic features.

- Ion-enhanced inhibitor. The inhibitor species form a polymer-like material on the sidewall that help to block etching of the sidewall and leads to increased anisotropy. It differs from Ion-enhanced energetic mechanism is that the chemical etching reaction takes place spontaneously even without ion bombardment. Neutral etchant species from the plasma spontaneously gasify the substrate, and ions play a role by interaction with another component – a "protective" inhibitor film.[9] The role of ions in here is to clear the inhibitor from horizontal surfaces that are bombarded by the flux of ions impinging in the vertical direction. The protective film is not removed from the vertical walls of masked features because these surfaces only intercept those few ions that are scattered as they cross the sheath. This protective film may originate from involatile etching products or from film-forming precursors that adsorb during the etching process.[8]

The ion-assisted plasma etching including ion-enhanced energetic and ion-enhanced inhibitor is the typical mechanism of most dry etching techniques widely used in VLSI development and manufacturing.

2.3 Dry Etching Equipment

The dry etching equipment can be divided two categories: Batch system and single-wafer etchers. We are only going to discuss the single-wafer etch system since they are more favored in the IC industry. Reactive Ion Etching (RIE) is commonly used for the fabrication of ICs. This kind of dry etching technique utilizes both the chemical and physical components of an etch mechanism. RIE tool is typically performed at 10 to 100 mTorr pressure in an asymmetric parallel-plate reactor and is highly anisotropic which means the vertical etch rate far exceeds the lateral etch rate. As shown in Figure 10, the area of a flat electrode holding the wafers is much smaller than the other electrode (>2:1). The smaller electrode is powered by rf power (radio-frequency, usually 13.56 MHz).[8] The reason that glow discharge processes operate at 13.56 MHz is that the international communications authorities designate this frequency where one can radiate a certain amount of energy without interfering with communications.[13] As discussed before, the medium-density plasma etcher that we are using is also called Dipole Ring Magnetron (DRM) and is operated at medium pressure. It can provide higher etch rate, higher selectivity, lower contact resistance, high repeatability for dielectric etching application. However, Plasma-Induced Damage (PID) needs to be considered for the performance of the devices. The high-density plasma etcher has dual frequencies that allow one to combine the advantages of the different frequency values. It is considered to

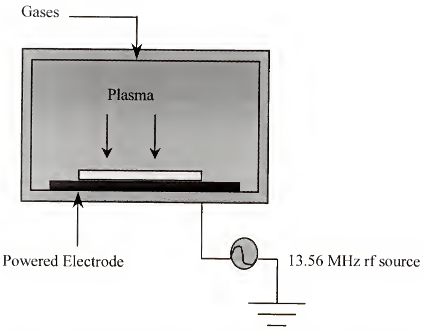


Figure 10. General configuration of a Reactive Ion Etching (RIE) etching system

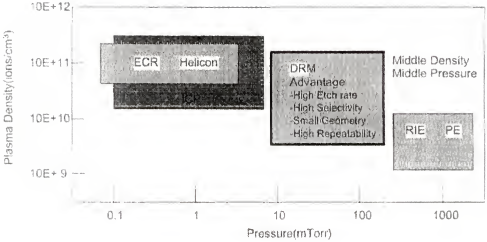


Figure 11. Plasma density vs Pressure for different etching systems

be the next generation etch tool that can sustain deeper feature size down to 0.08 μm technology. Using a higher frequency (60 MHz) on the upper electrode allows a high excitation of gas molecules, whereas a lower frequency (2 MHz) on the substrate electrode controls the energy of ion bombardment. High etch rate, good process repeatability and higher selectivity of SiO_2/SiN can be obtained in high-density plasma etching system. The plasma density is 1 to 2 orders of magnitude higher than DRM thus improving the bond breaking efficiency and the sputter desorption of etch products for the surface (see Figure 11). Therefore, this high-density plasma tool has more advantages to etch higher aspect ratio dielectric materials especially for SAC etch process. Additionally, Plasma-Induced Damage can be minimized without the magnetic field. However, particle control is a potential issue for manufacturing.

Table 1 shows the differences between DRM and high-density plasma etching tool. It is obvious that high-density plasma etching tool has bigger chuck temperature control, bigger vacuum pump, and better etch rate uniformity control because of the adjustable gap.

Table 1 - Comparison between Dipole Ring Magnetron (DRM) and high-density plasma etcher

	Gap (mm)	RF (MHz)	Magnet	Chuck Temp. (°C)	Vacuum pump size (liter/sec.)
DRM	27 (fixed)	13.56	Yes	-10 to 60	800
High-density plasma etcher	15 to 45 (adjustable)	60/2 (upper/lower)	No	-30 to 60	1200

There are other types of high-density plasma etch tools that are used in the VLSI industry frequently. One is called Electron Cyclotron Resonance (ECR) and another one is Inductively Coupled Plasma (ICP). Both of them can offer anisotropic etching at lower pressure for higher aspect ratio materials. Longer mean free path lengths of gas molecules and ions due to the lower pressures can reduce the scattering collisions. High ion density sources are designed to more efficiently couple input power with the plasma, resulting in greater dissociation of etch species. The main difference between ECR and ICP is that ECR employ an external magnetic field to shape and contain the plasma, while ICP sources do not.[9, 14] Figure 12 and 13 show the schematics of ECR and ICP etching systems respectively.

In ICP system, RF current, driven at 2 MHz, is supplied to the three coils in opposite directions and causes an alternating magnetic field in the upward and downward directions. It is the rate of change of this magnetic field that induces a rf electric field that confines and accelerates electrons in a circular path. This inductive coupling is very efficient and leads to a high-density plasma. Since the electrons are "trapped" in a circular path they have little chance of reaching the sample chuck that results in a low dc self-bias. Another rf source, driven at 13.56 MHz, is applied to the chuck which can control the dc bias. This allows near independent control of both ion flux (ICP power to the coils), and ion energy (rf power to the chuck). Since ICP tools do not use microwave sources or magnets for collimating the plasma, they offer advantages such as easier tuning and lower cost of ownership. ICP, as well as other high-density tools, offers much higher etch rates due to the large concentration of ions and radicals. Also, since the electrons are relatively confined, fewer electrons are lost to the walls or electrode compared to RIE, resulting in a lower dc bias and less ion damage. High-density tools also operate at much lower process pressures than low-density tools. Lower pressures

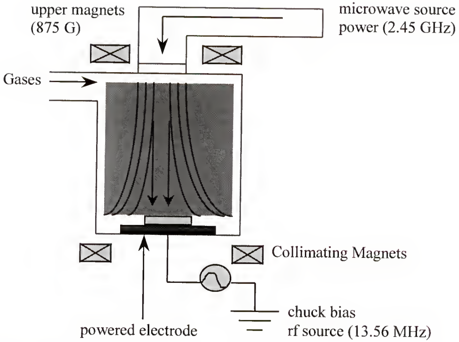


Figure 12. Schematics of Electron Cyclotron Resonance (ECR) etcher

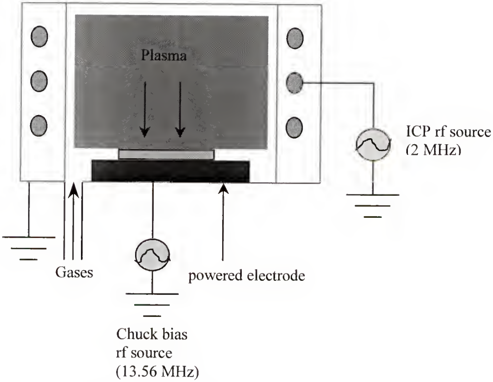


Figure 13. Schematics of Inductively Coupled Plasma (ICP) etcher

increase the mean free path of the particles that reduces gas-phase collisions and makes it possible to produce anisotropic etching.[18]

2.4 Further Discussion for Plasma Etching

2.4.1 Plasma Chemistries

Fluorinated chemistries are very popular in the plasma etching process. Table 2 summarizes some important chemical and physical processes that occur in a plasma etching process.

Table 2 - Some important chemical and physical processes

Reaction	Example
Positive ionization	$Ar + e \rightarrow Ar^+ + 2e$ $O_2 + e \rightarrow O_2^+ + 2e$
Dissociative ionization	$CF_4 + e \rightarrow CF_3^+ + F + 2e$
Fragmentation	$CF_3Cl + e \rightarrow CF_3 + Cle^-$ $C_2F_6 + e \rightarrow 2CF_3 + e$
Dissociative attachment	$CF_4 + e \rightarrow CF_3 + F^-$
Dissociative ionization with attachment	$CF_4 + e \rightarrow CF_3 + F^- + e$
Excitation	$O_2 + e \rightarrow O_2^* + e^-$
Photoemission	$O_2^* \rightarrow O_2 + h\nu$

O_2^* is the excited state of O_2.

In VLSI fabrication, it is very important to choose appropriate plasma chemistries for etching Silicon, SiO_2 and SiN in order to achieve anisotropy, good selectivity and etch rates. Generally, fluorocarbon plasmas are employed such as CF_4, C_4F_8, C_5F_8, mixtures of $CF_4 + O_2$. These source gases can have a significant effect on the concentration of a reactive neutrals and ions generated in the plasma thus affecting the etch characteristics.[10] The additive gases like Ar can stabilize the plasma, dilute etchants, and improve selectivity.[15] The ratio of chemical and physical of the etch mechanism also can be balanced by the gas additives. The dry etching reaction of SiO_2 may have the following steps.[16]

$$CF_4 + e^- \Rightarrow CF_x + F + e^-$$
$$CF_x + SiO_2 \Rightarrow SiF_4 + (CO, CO_2, COF_2)$$

The etching of Si may follow:

$$Si + CF_x \Rightarrow \text{C absorbed on Si}$$
$$Si + 4F \Rightarrow SiF_4$$

A mechanism for the F-atom reaction with a Si film leading to gasification products is summarized in Figure 14. The SiF_2 does not readily desorb since it is chemically bonded to the wafer. Impinging F atoms must penetrate this layer in order to be able to attack subsurface Si-Si bonds. Such penetration and bond breaking by F atoms apparently occurs, and continues by reducing the Si-Si bonds until a SiF_4 entity is formed. SiF_4 can desorb from the surface with minimum energy since no more bonds connect it to the Si lattice.[7]

If small concentrations of O_2 are added to the CF_4 feed gas, the etch rates of both Si and SiO_2 are observed to dramatically increase (see Figure 15). At low O_2 concentration (<15%), the selectivity of Si/SiO_2 is increased because O atoms reacts with CF_4 and more free F atoms are given.

$$CF_4 + O \Rightarrow COF_2 + 2F$$

At higher O_2 concentration (>15%), the selectivity of SiO_2/Si is increased because O atom absorbs free F atoms and the amount of free F atoms is reduced.

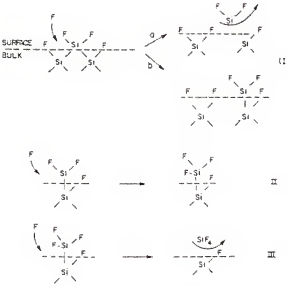


Figure 14. Proposed mechanisms for F-atom reaction with a Si film leading to the products SiF_2 and SiF_4

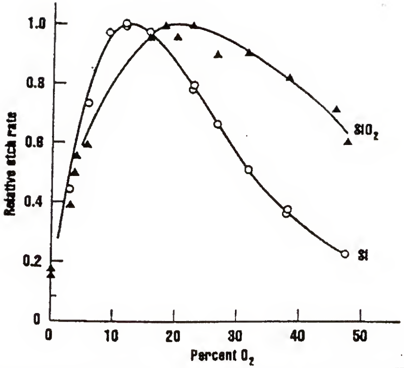


Figure 15. Etch rates of Si and SiO_2 vs the O_2 concentration in a CF_4-O_2 plasma

$$O_2 + F \Rightarrow FO_2$$
$$FO_2 + F \Rightarrow F_2 + O_2$$

The Fluorine-to-Carbon ratio model evolved to assist in assimilating the large amount of information on chemical and physical mechanisms observed in plasma etching. The model represents an attempt to organize such information into a framework that allows processes to be developed more efficiently, by providing some basis for predicting the effects of various parametric variations. Increasing the F/C ratio increases Si etch rates, and decreasing the F/C ratio lowers them.[7] In addition, the addition of O_2 has the effect of increasing the F/C ratio because O_2 consumes more carbon than F atoms. As shown in Figure 16, the boundary between polymerization is shown to vary as a bias voltage is applied to the substrate. The bias voltage has the effect of causing increased bombardment of the surface by energetic ions, which removes the deposited polymer layer by sputtering. This allows etching to occur at lower F/C ratio. If F/C >3, the etch occurs isotropically; if F/C <3, the sidewalls are protected by an inhibitor film, but ion bombardment exposes the bottom of the trench to the etchants, and this will produce highly anisotropic etching.[7, 17]

2.4.2 Etching Parameters

In VLSI fabrication industry, there are several etching parameters that are very critical for developing the etching processes. They are:

- Selectivity. This refers to the relative etch rate of the film to be etched to the etch rate of another material exposed to the etchant such as selectivity of SiO_2 over TiN. There are two types of selectivity, one with respect to the masking materials (Photo-Resist) and the other with respect to an underlying film. High selectivity with respect to both layers is needed to produce the required pattern resolution with minimal erosion of the mask and attack of the underlying film and other exposed materials.

- Plasma damage. Wafers in the plasma are exposed to energetic particle and photon bombardment. The radiation consists of ions, electrons, ultraviolet photons, and soft

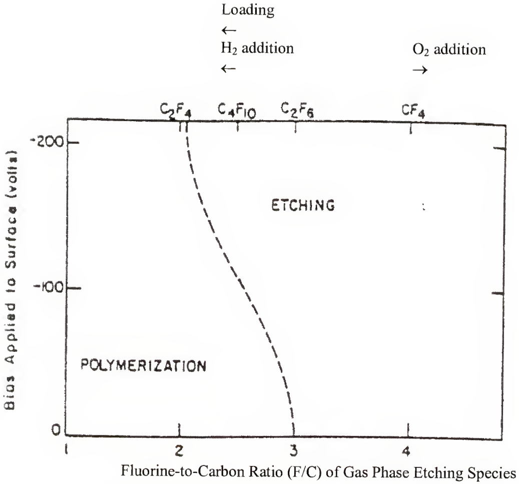


Figure 16. Boundary between polymerization and etching conditions as influenced by the fluorine-to-carbon ratio of the chemically reactive species and the bias applied to a surface in the discharge

X-rays. When high-energy radiation strikes the wafer surface, it can cause both shallow and deep surface disruption, which alters electrical characteristics and degrades device performance. Theoretically, lower power will reduce the plasma damage in dielectric materials etching. The damage can usually be detected as a change in the Capacitance-Voltage (CV) signature of Metal Oxide Semiconductor (MOS) capacitors, or gate leakage, lifetime and other operating parameters of the transistors.

- Microloading. It happens when the etch rate decreases as the exposed area of the wafer surface is increased. In VLSI industry, it is also defined by the ratio of the etch rate of blanket oxide wafer to the etch rate of pattered oxide wafer. The ratio is around 3:4 by using MERIE tool.

CHAPTER 3
ETCHING PROCESS FOR REGULAR CONTACT

3.1 Introduction

The procedure of the process check needs to be discussed first because it is very important to know the status of the machine and check the stability of the tool before any development experiments.

Two blanket oxide (without pattern) wafers are used for the regular process check. The pre-measurement of the thickness of the oxide layer and pre-particle count need to be collected on Thermo-Wave (San Jose, CA, USA) and Tencor (San Jose, CA, USA) analytical tools. Then the wafers are etched on the medium-density plasma etcher by using proper process check recipe. The post-particle data is collected immediately in order to reduce the error from the environment. Finally, the thickness of oxide remaining can be done on Thermo-Wave. The specification of particle adders should be less than 50 counts, and the thickness of the oxide remaining should be between 2400 Å to 2800 Å. The development experiments can be started after the process check is passed. Otherwise, the chamber has been cycled by using one PR lot. The wet clean has to be executed if the process check failed 2 to 3 times.

The design rules for 0.18 μm and below technologies are the diameters for contact holes and are less than 0.20 μm. Figure 17 shows the film stacks of the regular contact: Deep Ultra-violet (DUV) Photo-Resist, very thin Spin Anti-Reflection Coating (SPARC) layer, Phosphorus Silicon Glass (PSG), Un-doped High Density Plasma (HDP) SiO_2. The total oxide depth is 1 μm and thus the aspect ratio for these two different

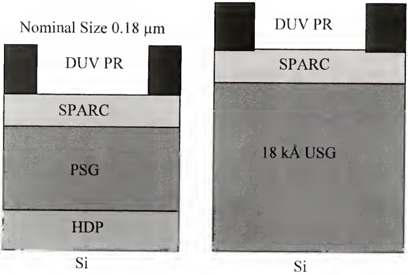


Figure 17. Film stacks for the regular contact

technologies are 5:1 and 5.6:1. Therefore, highly anisotropic etching is strongly desired due to the smaller feature size. In addition, higher selectivity of oxide/Si (> 30:1), tight CD control (inline range: ± 0.04 μm) after etching, 25 to 30% over-etch process margin and at least 88 to 89° taper angles are strictly required. Oxide etch depth (over-etch margin) was checked by using 18 kÅ Un-doped Silicon-Glass (USG) wafers those were pattered same as the 10 kÅ wafers by using the same reticule. The Si loss is measured on the cross-section pictures after the etched wafer is dipped in BOE solvent for 5 seconds. The interface layers between the oxide layer and Si layer can be distinguished clearly. In order to meet the above requirements, we used the medium-density plasma tool to develop the etching process and collect the electrical data from several lots. There are 25 wafers in a single lot in the industry. The electrical data on the split lots includes contact resistance, defect density, yield etc.. The process split covers process margin check such as 10% under etch and 10% over etch based on the final process, Chemical Mechanical Polish (CMP) variation margin check, and Photo-Resist evaluation. The pressure range of etching process is from 30 mT to 50 mT, the power range is from 1100 W to 1700 W, and gases C_4F_8, CF_4, Ar, CO, O_2 are used.

3.2 Evaluation of Baseline Recipe

The evaluation work for contact etching process was based on the following:

- Profile and over-etch margin. These are based on the cross-section pictures of the etched wafers. The diameter of the wafer is 200 mm. All of the Scanning Electron Microscope (SEM) pictures were taken both in the center and edge (around 10 cm away from the edge of the wafer) of the wafer. subnominal section (CD size is 0.02 μm smaller than the nominal size), nominal section, and supernominal section (CD size is 0.02 μm bigger than the nominal size) including isolated and nested areas also are investigated. Figure 18, Figure 19, and Figure 20 show the etch profiles in isolated and nested areas in subnominal section, nominal section, and supernominal section respectively. The top and bottom CDs are in the specification after etching. It

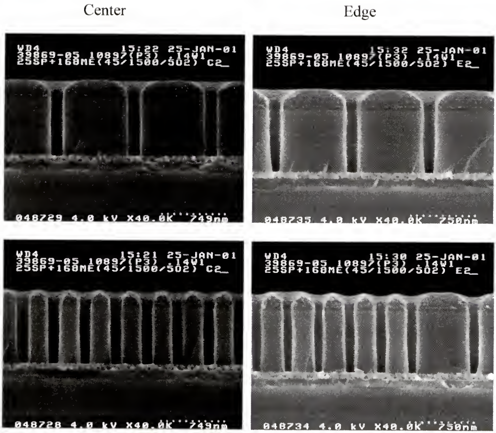
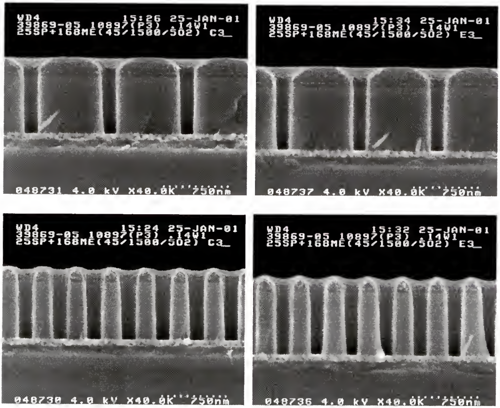

Center
Edge
WD4 15:22 25-JAN-01
39869-05 10897(P3) .14W1
25SP+168ME(45/1500/502) C2
048729 4.0 kV X40.0K 749nm
WD4 15:32 25-JAN-01
39869-05 10897(P3) .14W1
25SP+168ME(45/1500/502) E2
048735 4.0 kV X40.0K 750nm
WD4 15:21 25-JAN-01
39869-05 10897(P3) .14W1
25SP+168ME(45/1500/502) C2
048728 4.0 kV X40.0K 749nm
WD4 15:30 25-JAN-01
39869-05 10897(P3) .14W1
25SP+168ME(45/1500/502) E2
048734 4.0 kV X40.0K 750nm

Figure 18. Cross-sections of contact in subnominal section
(Note: top – isolated areas, bottom – nested areas.)



Center

Edge

WD4 15:26 25-JAN-01
39869-05 10897(P3) .14W1
25SP+168ME(45/1500/502) C3_
048731 4.0 kV X40.0K 750nm
WD4 15:34 25-JAN-01
39869-05 10897(P3) .14W1
25SP+168ME(45/1500/502) E3_
048737 4.0 kV X40.0K 750nm
WD4 15:24 25-JAN-01
39869-05 10897(P3) .14W1
25SP+168ME(45/1500/502) C3_
048730 4.0 kV X40.0K 750nm
WD4 15:32 25-JAN-01
39869-05 10897(P3) .14W1
25SP+168ME(45/1500/502) E3_
048736 4.0 kV X40.0K 750nm

Figure 19. Cross-sections of contact in nominal section

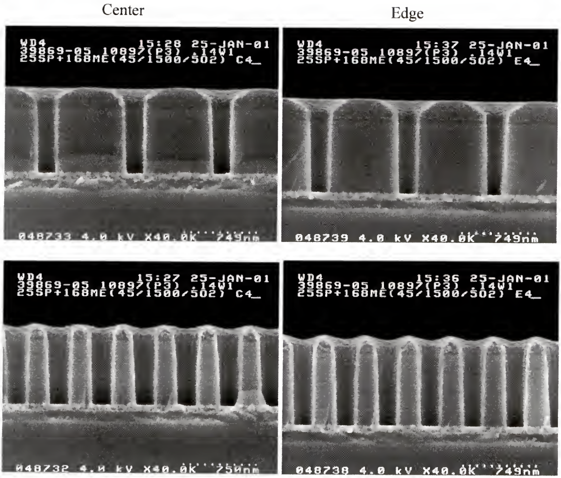

Center
Edge
WD4 15:28 25-JAN-01
39869-05 10897(P3) .14W1
25SP+168ME(45/1500/502) C4_
048733 4.0 kV X40.0K 749nm
WD4 15:37 25-JAN-01
39869-05 10897(P3) .14W1
25SP+168ME(45/1500/502) E4_
048739 4.0 kV X40.0K 749nm
WD4 15:27 25-JAN-01
39869-05 10897(P3) .14W1
25SP+168ME(45/1500/502) C4_
048732 4.0 kV X40.0K 750nm
WD4 15:36 25-JAN-01
39869-05 10897(P3) .14W1
25SP+168ME(45/1500/502) E4_
048738 4.0 kV X40.0K 749nm

Figure 20. Cross-sections of contact in supernominal section
(Note: top – isolated areas, bottom – nested areas.)

indicates the pattern is transferred smoothly when the baseline process is used. The taper angle can be calculated by the following formula:

Taper Angle = arc tangent [(top CD – bottom CD)/oxide depth]

Based on the etching profile, a taper angle 88.7° is obtained which meets the requirement. Over 30% over etch has also been obtained by using 18 kÅ USG wafers. Figure 21 shows 13.9 kÅ etch depth.

- Selectivity. Two types of selectivity are studied for the regular contact etching process. One is the selectivity of SiO_2 over Photo-Resist (PR), and another one is the selectivity of SiO_2 over Si. The thickness of PR before etching needs to be measured based on the cross-section SEM pictures of incoming wafer (just before contact etching), and the thickness of remaining PR also needs to be obtained from the SEM pictures after etching. The difference is the PR loss during etching. The etch rate of PR is the quotient of PR loss divided by etching time. The quotient of the total oxide etch depth divided by the etching time is the etch rate of SiO_2. Therefore, selectivity of SiO_2 over PR is equal to etch rate of SiO_2 over etch rate of PR. The selectivity of SiO_2/PR is around 6:1 in contact etching process. This guarantees the PR margin is enough when the over etching is about 30%. By applying the same method, the selectivity of SiO_2 over Si can be calculated too.

  Selectivity of SiO_2/Si = Etch rate of SiO_2/Etch rate of Si

  The high selectivity of SiO_2/Si can be up to 35:1. This indicates a bigger process margin for Si gauging and fully meets the integration requirement.

- The Si loss. Figure 22 shows the cross-section SEM pictures of the etched wafer that has been decorated by 5 seconds BOE treatment. The Si loss is about 130 Å in the nominal section that meets the integration requirement completely.

3.3 Final Process

The electrical data are collected in order to further evaluate the baseline recipe.

There are 5 full-loop lots that are split to check the process margin as the following:

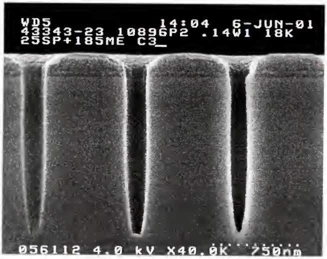
POR (Process of Record, baseline process)

+10% Over Etch (+10% extra Main Etch time)

+20% Over Etch (+20% extra Main Etch time)

The process margin has been checked by extra etch time because the medium-density plasma etcher does not have the endpoint system. The responses of the split lots are

Center



Edge

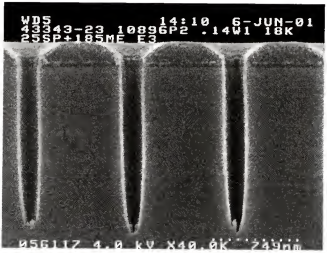
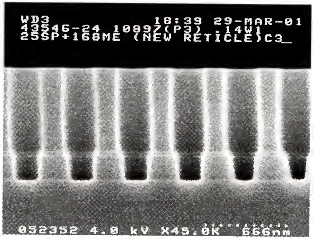


Figure 21. Cross-sections of contact for over etching study

Center



Edge

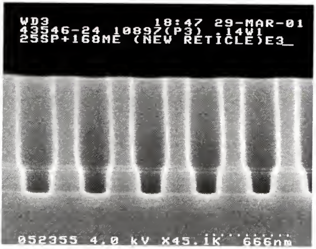


Figure 22. Cross-sections for Si loss in contact etching process

contact resistance of P-channel and N-channel, defect density, gate leakage, and yield. Another contact etching process is developed to check the limit of the process. It is called delicate contact etching and has more aggressive over etching. During this process, one more etch step is added after +10% Over Etch process by applying higher pressure, much lower power and different gas chemistries such as CH_2F_2. The purpose of this extra etch step is to generate more polymers to gently land on the gate and maintain enough over etching. The results from the several split lots show the current Process of Record (POR) still has enough process margins although the delicate contact etching process shows the similar electrical result as the POR cell.

Finally, the baseline process is qualified to transfer to the manufacturing lines. However, the split between the manufacture tool and development tool needs to be done for comparison before qualification. Then the contact etching process is completely implemented in the production line based on the comparable electrical data from the split lots.

CHAPTER 4
ETCHING PROCESS FOR REGULAR VIAS

4.1 Introduction

The process check needs to be done at least 3 to 4 times per week for the manufacturing tool and once a week for the development tool. The procedure of the process check has been described in Chapter 3.

The diameters of the vias for 0.18 µm and below technologies are less than 0.24 µm, corresponding to aspect ratios of 4.5:1. The film stacks of vias are very similar with the film stacks of contact (see Figure 23). The thin films are: Deep Ultraviolet (DUV) Photo-Resist, very thin Spin Anti-Reflection Coating (SPARC) layer, Silicon Rich Oxide (SRO), and Fluorine Silicon Glass (FSG).

The over-etch margin is still checked by using 18 kÅ USG wafers. Additionally, the etch process must stop on the TiN layer required by the integration design. Certainly, the same medium-density plasma etcher (Magnetic-Enhanced) are used as the contact etching process does. The advantage of this MERIE etcher is the high uniformity because a dipole ring magnet rotates around the reactor. Plus, the reactor is equipped with Electrostatic Chucks (ESC).[23-33]

Therefore, the following requirements need to be satisfied:

- Selectivity of oxide/TiN: >20:1
- CD control: inline range (±0.04 µm) after etching
- Over-etch process margin: 40 to 50% over-etch to stand the CMP variation
- Taper angles: 87 to 89°

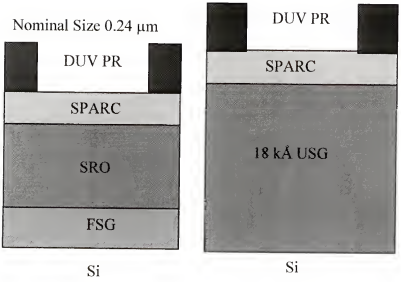


Figure 23. Film Stacks of vias

The reason why the over-etch process margin should be wider than the regular contact etching process is that the topographic variation becomes bigger as the metal levels increase. In addition, the selectivity of SiO_2 over TiN must be addressed extensively because the Electron Migration (EM) would be several orders worse if the TiN layer is punched through.

The electrical characterization is done after a standard metallization scheme (back-sputtering, TiN barrier, and W plugs). The electrical data on the split lots include contact resistance, defect density, yield etc.. The process split covers process margin check such as 10% under etch and 10% over etch based on the final main etching time, Chemical Mechanical Polish (CMP) variation margin check, and Photo-Resist evaluation. The pressure range of etching process is from 30 mT to 50 mT, the power range is from 1100 W to 1700 W, and gases C_4F_8, CF_4, SF_6, Ar, CO, O_2 are used.

DOE needs to be done in order to find the key parameters for the via etching process. It is also a good reference for the contact etching process. The main etch parameters are Pressure, Power, and Gas flows for C_4F_8 and O_2. Uniformity, over-etch process margin, and final CD are predicted accurately based on DOE results.

Plasma-Induced Damage (PID) needs to be investigated among different etchers and different etch processes for contact and via etching processes. Theoretically, lower power will reduce the plasma damage. Plus, the thickness of gate oxide is another important factor for the plasma damage in the back end of line. The thicker the gate oxide is, the less the amount of plasma damage caused by dielectric etching processes.

4.2 Evaluation of Baseline Recipe

The evaluation work for the regular via etching process is much more complicated than the regular contact etching process, since the requirements are much stricter from the integration viewpoints and the variation of the dielectric layers becomes wider as the window levels increase. Therefore, the baseline recipe needs to be investigated intensively in order to deliver more robust etching process to the production lines. The baseline process is divided by two steps: SPARC etching and Main etching.

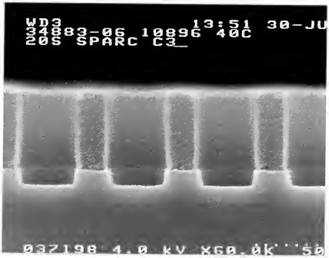
4.2.1 Spin Anti-Reflection Coating (SPARC) Etching Study

The SPARC layer used by the photolithography engineer is to improve the photo process margin in order to print very small via holes on the wafers. This layer is very thin (Approximate to several hundreds Anstrongs). Therefore, the different etching chemistries are used for this step in order to breakthrough SPARC layer in a short time and maintain the small CD . CF_4 is used instead of C_4F_8 because higher F/C ratio is more helpful to breakthrough the SPARC layer. There are three parameters that we must understand very well when the SPARC etching step is studied:

- CD maintenance. This means that the via size must be maintained and the variation range must be less than ±0.02 μm. Otherwise, the final CD will be out of the required range after the long time main etching.
- Oxide loss. This has to be kept in the smallest range because more oxide loss will cause more Photo-Resist loss. The selectivity of Photo-Resist to oxide is around 1:1 which means the same amount of Photo-Resist will be lost as the same amount with oxide loss. Plus, too much oxide loss will increase the cycle time due to the longer etching time.
- Photo-Resist remaining. It must be preserved as many as we can since much more Photo-Resist is consumed quickly for the following main etching process. Otherwise, the top CD will blow up and the straight profile cannot be maintained.

Figure 24 shows the cross-sections of standard SPARC etching process. The pictures are taken on both of center and edge of the wafer. The problem for the standard SPARC etch step is that CD is decreased prior to main etching process. It causes that the final inline CD is always smaller than the specification. Additionally, there are more

Center



Edge

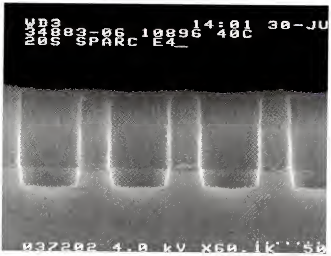


Figure 24. Standard SPARC etching process

potential chances to have the etch stop for the subnominal vias due to the reduced CD in the beginning of main etching. Therefore, it is very necessary to investigate the SPARC etching process carefully by adjusting the SPARC etching time.

First of all, the incoming data needs to be collected in order to have the reference before we start to study the SPARC etching step. It is also very important to know the variation during the photolithography step before the etching experiment. Usually, the inline CD is the average number of the measurements on the 9 sites. The chip number and wafer map is shown in Figure 25. The measurement work is done on the Hitachi-9400 that is a top-down CD measurement tool. The biggest advantage to use the Hitachi-9400 is that the image data can be collected without cleaving the wafer. It saves the money for wafer cost and the time for cross-section. Therefore, the Hitachi-9400 is widely used inline to monitor the CD variation before and after etching process very well. The only shortcoming of this tool is that it cannot provide the via profile information. The 3-Dimensional (D) top-down CD SEM tool is developing according to the latest report. Both the profile and top-down information can be obtained in the near future by using the 3-D top-down CD SEM tool. The ownership cost is reduced significantly since more wafers can be saved without cleaving. Figure 26 shows the top-down CD SEMs on the wafer that is ready to be etched inline. The pictures are taken on both of isolated and nested sections of vias for comparison. The inline CD, Photo-Resist thickness, uniformity can be checked based on these pictures.

Secondly, the experiment is designed by increasing the SPARC etch time because the bigger final CD is required. Therefore, the different etching times – 20 seconds, 25 seconds, and 30 seconds are set up. The top-down CD SEM and cross-section SEM are

site	x	y
1	1	4
2	3	2
3	3	6
4	4	1
5	4	4
6	4	7
7	6	2
8	6	6
9	7	4

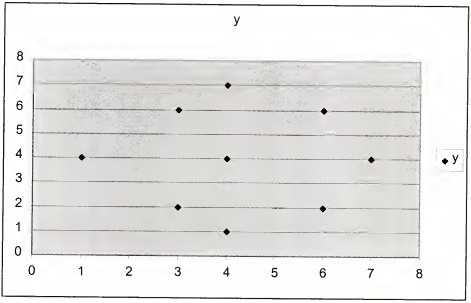
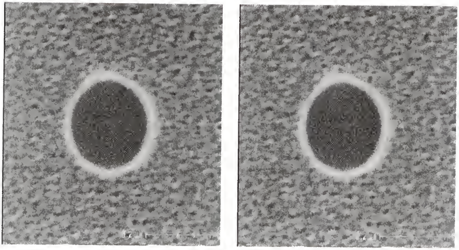


Figure 25. Wafer map for the inline Critical Dimension (CD) measurements

Center

Isolated Nested



Edge

Isolated Nested

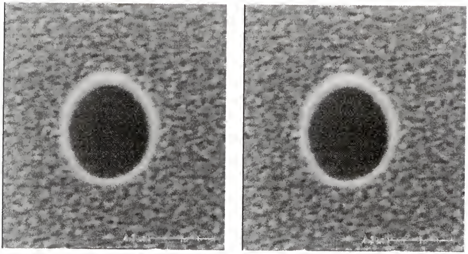


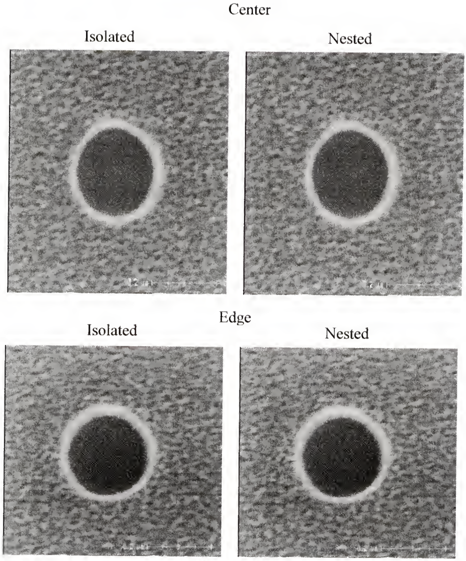
Figure 26. Top-down CD SEMs for the incoming wafer

evaluated before and after SPARC etching. Figure 27, Figure 28, and Figure 29 show the top-down CD SEM pictures for 20 seconds, 25 seconds, and 30 seconds SPARC etching time on the center and edge of the wafer respectively. The SPARC layer has been punched through and the tiny variation of top-down CD is obtained for all of the different SPARC etching times. Compared with the standard SPARC etching process, the process of 25 seconds etching can provide bigger final CD and maintain similar Photo-Resist remaining. The process of 30 seconds etching causes too much oxide loss and Photo-Resist consuming and reduces the Photo-Resist margin of main etching. Therefore, the standard SPARC etching process is modified and increased 5 more seconds in order to meet the advanced integration requirement. Figure 30 compares the difference between Defined Inspection Critical Dimension (DICD) and Final Inspection Critical Dimension (FICD) for the above experiments. Figure 31 shows the cross-section SEM pictures for three different processes. The oxide loss and Photo-Resist remaining can be measured easily by using the PCI software.

Finally, the split lots need to be run among the different SPARC etching times to see the effect of the electrical data. The 25 seconds SPARC etching process is implemented to the routing eventually because several split lots shows better electrical data than the previous Process of Record (POR) process. The process margin check for the SPARC etching step is finished completely.

4.2.2 Main Etching and Over Etching Studies

There are two different directions for via etching process. One is called "Break-through (BT)" which means the TiN layer is broken through after via etching.



Center

Isolated

Nested

Edge

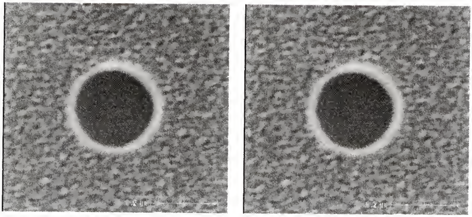
Isolated

Nested

Figure 27. Top-down CD SEM pictures for 20 seconds SPARC etching

Center

Isolated Nested



Edge

Isolated Nested

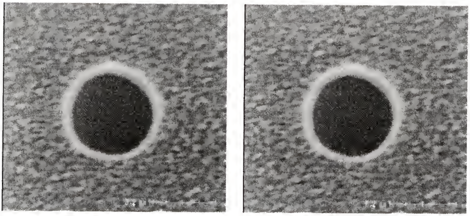
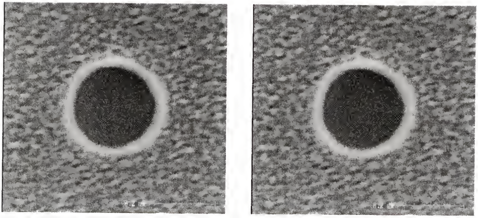


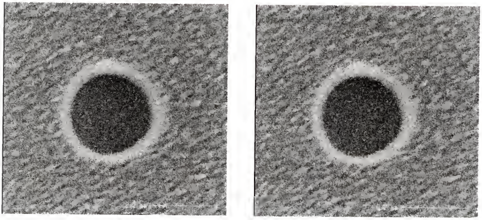
Figure 28. Top-down CD SEM pictures for 25 seconds SPARC etching



Center

Isolated

Nested

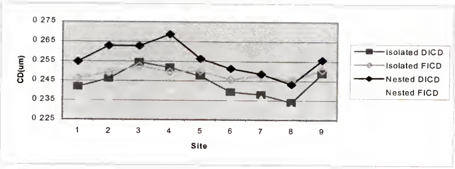


Edge

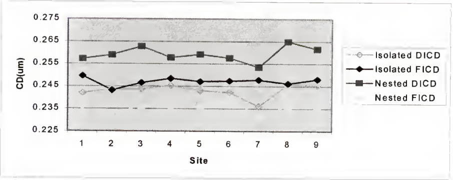
Isolated

Nested

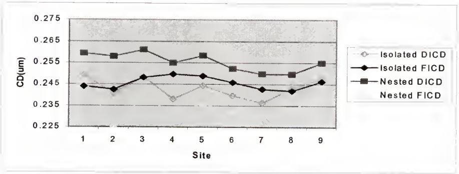
Figure 29. Top-down CD SEM pictures for 30 seconds SPARC etching



20 seconds SPARC etching

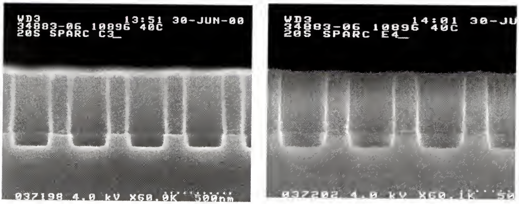


25 seconds SPARC etching

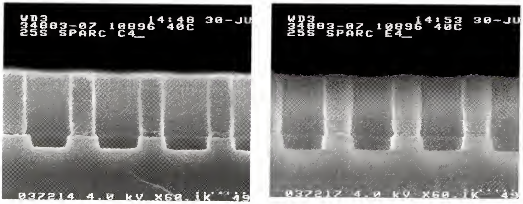


30 seconds SPARC etching

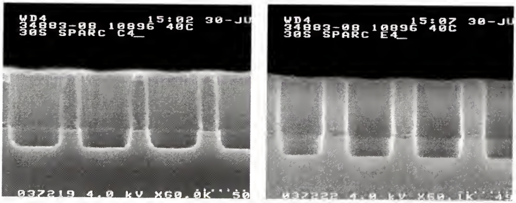
Figure 30. Comparison between Defined Inspection Critical Dimension (DICD) and Final Inspection Critical Dimension (FICD)



20s SPARC oxide loss C/E (nm): 86/90



25s SPARC oxide loss C/E (nm): 89/93



30s SPARC oxide loss C/E (nm): 133/137

Figure 31. Cross-section SEM pictures for three different SPARC processes

Another one is called “Stop on TiN” which means that the TiN layer cannot be punched through after main etching. The following discusses these two processes respectively:

- BT process. Originally, this process was evaluated due to its simplicity because the selectivity of oxide over TiN is not critical. In fact, lower selectivity is required in order to break-through the TiN layer completely. This process has three etching steps: SPARC etching, Main etching, and TiN break-through steps. CF_4 was used in the TiN break-through step first. However, higher contact resistance is obtained by using CF_4 break-through process. Therefore, the similar gas chemistries ($C_4F_8/O_2/Ar/CO$) are used both in main etching and BT steps to reduce the contact resistance.

  The modified BT process can provide more over-etch margin for the variation of dielectric layers during CMP step since the gas chemistries etch away both oxide and TiN layers. In order to break-through TiN completely and gentlely, lower power, higher pressure, and longer etching time are also applied during modified BT step. Figure 32 shows the cross-sections of via after W plugs deposited by using same gas chemistries in both main etching and BT steps. The taper angle of via profile is around 88.6°, CD bias that means the difference between DICD and FICD is about 0.01 μm, the Aluminum (Al) gauging is about 58 nm.

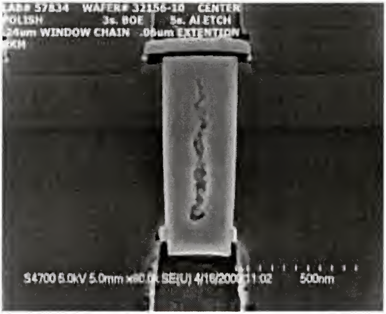
  The third approach is also investigated for TiN break-through step by using SF_6 gas chemistry. Much lower power, higher pressure, shorter etching time compared to main etching are applied for the SF_6 break-through step. However, this process causes too much Al gauging which increases the contact resistance. Figure 33 shows the cross-section of via profile for SF_6 process after W plugs deposited. Finally, the C_4F_8 TiN break-through process shows the least contact resistance among the three different approaches on several split lots. Therefore, this process is fixed inline as the POR process for TiN break-through application. All of the above work is completed on the development tool.

  As high volume manufacture is demanded, more chambers that are the same model with the development chamber are purchased. The qualification for the new chamber is finished after the C_4F_8 BT process is implemented inline. The procedure of the qualification on the manufacturing tool is as follows:

  - The mechanical check on the new chamber. It includes the installation work on the new chamber, standard process check to verify the etch rate and particle adders with the development chamber. The etch rate and particle adders on the new chamber must match the data collected on the development chamber.

  - Process match. The patterned contact and via wafers including 18 kÅ wafers need to be etched on the new chamber by using the exact recipe as the development tool. The cross-section SEM pictures must be compared one by one to check the etch profile, etch depth, CD, taper angles, and Photo-Resist remaining. All of the responses must match each other on the different tools.

Center


LAB# 57834 WAFER# 32156-10 CENTER
POLISH 3s. BOE 5s. Al ETCH
.24um WINDOW CHAIN .00um EXTENTION
S4700 5.0kV 5.0mm x80.0k SE(U) 4/16/2000 11:02 500nm

Edge

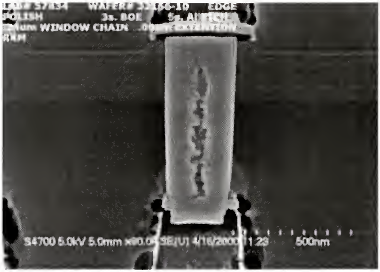
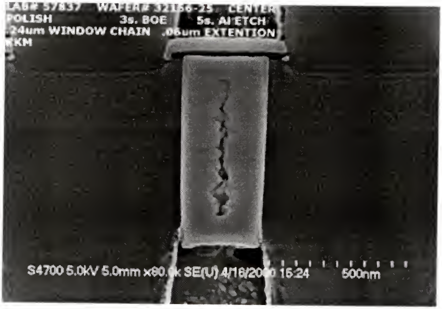


Figure 32. Cross-sections of Break-through (BT) process after Tungsten (W) plugs deposited

Center


LAB# 57837 WAFER# 32156-25 CENTER
POLISH 3s. BOE 5s. Al ETCH
.24um WINDOW CHAIN .06um EXTENTION
KM
S4700 5.0kV 5.0mm x80.0k SE(U) 4/16/2000 15:24
500nm

Edge

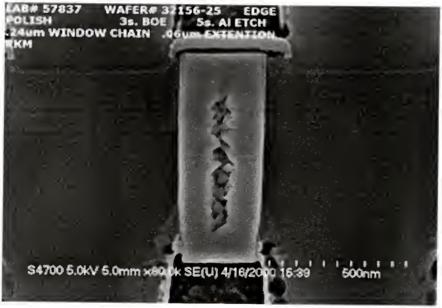

LAB# 57837 WAFER# 32156-25 EDGE
POLISH 3s. BOE 5s. Al ETCH
.24um WINDOW CHAIN .06um EXTENTION
KM
S4700 5.0kV 5.0mm x80.0k SE(U) 4/16/2000 15:39
500nm

Figure 33. Cross-sections of via for SF_6 process after W plugs deposited

The hardware of the new chamber needs to be checked if there is any unsatisfied difference between the two chambers.

  - Marathon on the new chamber. The purpose of the marathon is to check the repeatability of the process and the mechanical performance of the tool. The details is discussed in Chapter 5 when we develop the SAC etching process.

  - Electrical data. The lot can be split until the step b is satisfied. The half lot is etched on the development chamber, and another half lot is etched on the new chamber by applying the exact etching recipe. The split wafers are merged together after via etching. It is very important to keep this lot be only split at the via etching step in order to avoid some possible side-effect factors happened in other process areas. The new chamber can be brought up as a production chamber once the comparable electrical data is collected. In this case, one more split lot is preferable to be etched for repeatability.

- Stop on TiN process. The via etching process has to be changed to another direction — "Stop on TiN" according to the requirement from the integration side after the BT process has been running for 6 to 7 months. The reason is that the BT process causes more failure and reduces the lifetime of the device.

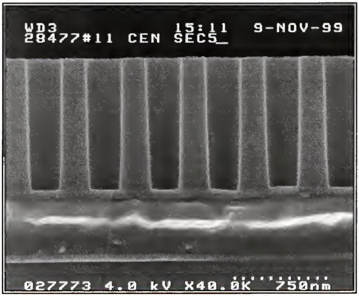
  On the other hand, the "Stop on TiN" process can improve Electron Migration (EM) that decreases the failure time tremendously. This new process is more difficult to develop than the BT process since much higher selectivity of oxide over TiN is required during via etching. However, the only drawback of the "Stop on TiN" process is that the contact resistance is 1 to 2 Ω higher than the BT process. The final decision is to develop the "Stop on TiN" process to replace the current BT process because "Stop on TiN" process can enhance the lifetime of the electrical devices dramatically.

4.2.3 Baseline Recipe

The baseline recipe for the "Stop on TiN" process is set up as the following: SPARC etch step, Main Etching step. It is also called one step etching process since the over etching is included in the Main Etching step.

During Main etching step, higher chuck temperature, lower power are explored to get higher selectivity of oxide to TiN in the beginning of development work. In addition, the thickness of TiN layer is doubled to have bigger etching process margin. Figure 34 shows the cross-sections of "Stop on TiN" baseline process. The via etching process is stopped on the TiN layer successfully and the via profile is shaped straightly. The TiN

Center



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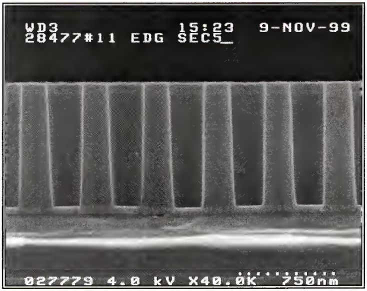
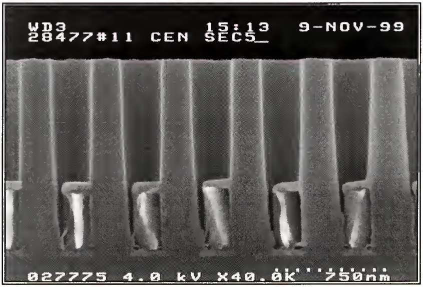


Figure 34. Cross-sections of “Stop on TiN” baseline process

gauging is around 12 nm/14 nm (center/edge) and equals 10% to 20% of the TiN thickness. The CD bias is less than ±0.01 μm that is very similar with the BT process. 40% to 50% over-etch without etch stop is obtained from the cross-section SEM pictures on 18 kÅ wafers. Much higher selectivity of oxide over TiN is up to 32:1 during the baseline process. It is very interesting to find another issue relative to the process margin of the photolithography step after the wafer is etched with the baseline etch recipe. The TiN layer is broken through at the corner of the vias due to the misalignment of the vias. The chance for the failure of EM is increased dramatically as the break-through process did before. Figure 35 shows the cross-section SEM pictures for the misalignment vias after etching and PR strip. Figure 36 shows the cross-section SEM pictures for the same misalignment vias after W plugs deposited. Both of them obviously indicated that the misalignment issue should be addressed before the lots go to via etch step. This problem is solved smoothly after the photo engineers adjust the process margin and reset up the speciation of the misalignment.

The special experiment is completed to check the etch rate of TiN during main etching. The method used in here is to have the difference of TiN gauging be divided by the difference of etch times. At first, some special mechanical wafers need to be prepared for the experiments. The bare Si wafers are used in here to reduce the development cost. The 1000 Å TiN layer is deposited on the Si wafers instead of standard TiN thickness. Then the wafers go through the standard Via Zone Test (VIAZT) routing to have the regular dielectric layer deposition and the standard photolithography process. The advantage of these mechanical wafers is that they are very similar with the actual VIAZT wafers except thicker TiN layer. The more accurate data can be collected on these wafers.

Center



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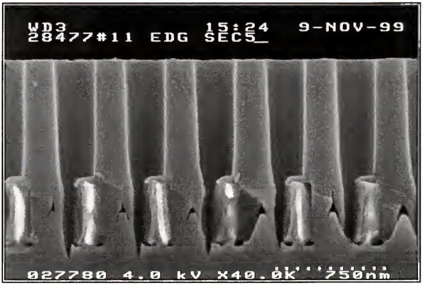
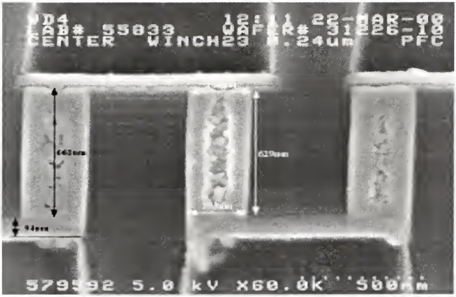


Figure 35. Cross-sections of "Stop on TiN" baseline process for the misalignment vias after etching

Center



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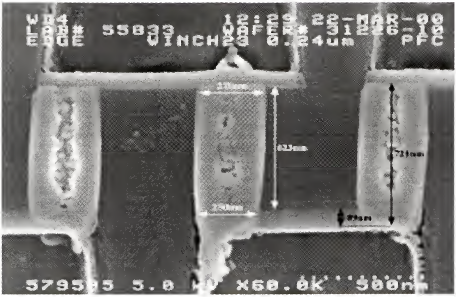


Figure 36. Cross-sections of “Stop on TiN” baseline process for the misalignment vias after W plugs deposited

Finally, one mechanical wafer is etched by using the baseline “Stop on TiN” process, another mechanical wafer is etched one more extra minute compared to the previous wafer. The difference of TiN gauging can be read accurately from the cross-section SEM pictures of these two wafers by using the PCI software. The etch rate of TiN can be calculated by the quotient of the difference of TiN gauging over one minute. The final TiN etch rate is about 150 Å/min which is very slow compared to the etch rate of oxide during the main etching. The selectivity of oxide over TiN is obtained after the etch rate of oxide is divided by the etch rate of TiN.

4.3 Design of Experiments (DOE)

4.3.1 First DOE

There is a big drawback for the baseline recipe. The chuck temperature has to be increased every time when the via lots are needed to be processed since the chuck temperature on the same chamber for the contact etching process is lower than the “Stop on TiN” baseline process. Both contact and via etching process share the same chamber because of the ownership cost. It means that the same chuck temperature has to be set up for both contact and via etching processes for the manufacturing requirement. Additionally, the same chamber is also used for SAC etching process that is asked lower chuck temperature. Therefore, the baseline recipe for “Stop on TiN” process has to be evaluated at lower chuck temperature although the higher chuck temperature can provide higher selectivity of oxide over TiN. It is very necessary to execute the first DOE in order to find the process margin at lower chuck temperature. Four key parameters are chosen for this DOE. The parameters are: chuck temperature, RF power, total gas flow, and C_4F_8/O_2 gas ratio. The two interested responses are: selectivity of oxide over TiN and etch depth. We know the TiN gauging margin by applying the selectivity of oxide over TiN, and the etch stop by studying the etch depth. The variation range is:

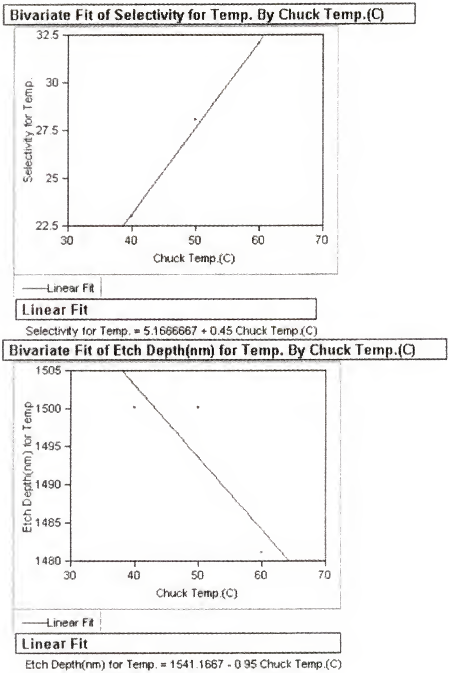
Chuck Temperature: 40 °C to 60 °C

RF Power: 1000 W to 1700 W

Total gas flow: 200 sccm to 340 sccm

C_4F_8/O_2 gas ratio: 2 to 2.5

There are 14 wafers that have been etched totally by following the above designs respectively. Only one parameter is changed for every run. The cross-sections are completed for all of the 14 wafers on the Hitachi-4500. Figure 37 shows the effect of chuck temperature. The selectivity of oxide over TiN is increased as the chuck temperature increases. The selectivity can be up to 32:1 when the chuck temperature is at 60 °C that is very consistent with our previous data. The selectivity of oxide over TiN is less than 30:1 on both 40 °C and 50 °C chuck temperature. The higher chuck temperature is very helpful to increase the selectivity of oxide over TiN during via etching. However, the etch depth is dropped obviously when the chuck temperature is increased to 60 °C. Compared with over 50% over-etch for 40 °C and 50 °C chuck temperature processes, there is only 45% over-etch can be obtained at 60 °C chuck temperature process. It indicates that lower chuck temperature is helpful to increase the etch depth. There is no etch stop shown on the etch front of the cross-section SEM pictures among three different chuck temperature. The process at 50 °C can provide a reasonable selectivity of oxide over TiN and up to 50% over-etch of etch depth. However, it still needs to change the chuck temperature prior to via etching as the 60 °C process does. The data tells us that higher chuck temperature can provide higher selectivity of oxide over TiN and less etch



Bivariate Fit of Selectivity for Temp. By Chuck Temp.(C)

Linear Fit

Selectivity for Temp. = 5.1666667 + 0.45 Chuck Temp.(C)

Bivariate Fit of Etch Depth(nm) for Temp. By Chuck Temp.(C)

Linear Fit

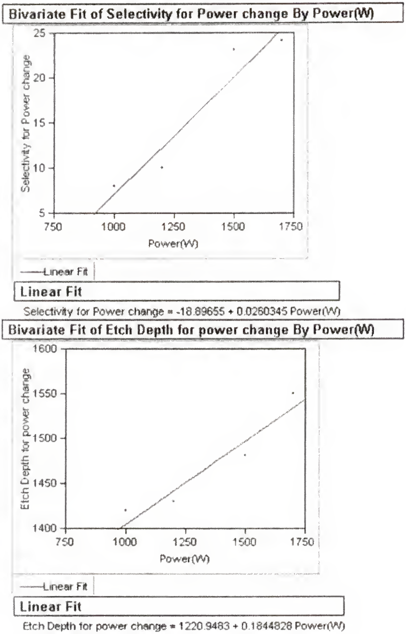
Etch Depth(nm) for Temp. = 1541.1667 - 0.95 Chuck Temp.(C)

Figure 37. Effect of the chuck temperature

depth that might cause etch stop easily. Another option is to change the chuck temperature of contact etching process and SAC etching process to 50 °C. For contact etching process, the POR process can be operated at 50 °C and meet the similar integration requirements. However, the current SAC POR process cannot meet the integration requirements since the etch stop happened at 50 °C. This small process margin is discussed in the Chapter 6 intensively. Therefore, the "Stop on TiN" process has to be fixed at 40 °C chuck temperature in order to satisfy the manufacturing requirements for three different applications. It is very challengable to develop the process at 40 °C chuck temperature because of the lower selectivity of oxide over TiN. The development work is discussed intensively in the following sections.

Figure 38 shows the effect of RF power. Both the selectivity of oxide over TiN and etch depth are increased when the RF power is increased. The selectivity is close to 10:1 when RF power is very low. The higher selectivity and etch depth are obtained (around 22:1, and 15 kÅ respectively) when RF power is around 1700 W. It indicates that the higher RF power is very helpful to increase the selectivity and etch depth simultaneously. However, this process cannot be chosen because the issue for higher power is that this process might cause the plasma damage seriously. Therefore, the medium-power process is chosen due to the reasonable selectivity and etch depth.

Figure 39 shows the effect of the total gas flow. The selectivity of oxide over TiN is decreased dramatically from 34:1 to 17:1 when the total gas flow is increased, and there is a peak point for the etch depth when the total gas flow is between 250 sccm and 300 sccm. The etch stop appears when the total gas flow is either less than 250 sccm or greater than 250 sccm. The etch depth is less than 14000 Å which means over-etch is



Bivariate Fit of Selectivity for Power change By Power(W)

Linear Fit

Selectivity for Power change = -18.89655 + 0.0260345 Power(W)

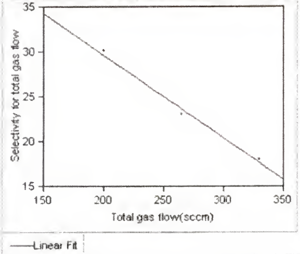
Bivariate Fit of Etch Depth for power change By Power(W)

Linear Fit

Etch Depth for power change = 1220.9483 + 0.1844828 Power(W)

Figure 38. Effect of RF power

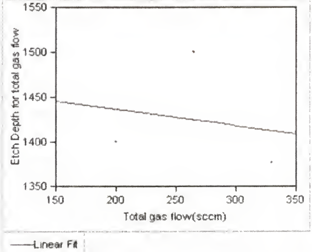
Bivariate Fit of Selectivity for total gas flow By Total gas flow(sccm)



Linear Fit

Selectivity for total gas flow = 48.128205 - 0.0923077 Total gas flow(sccm)

Bivariate Fit of Etch Depth for total gas flow By Total gas flow(sccm)



Linear Fit

Etch Depth for total gas flow = 1474.2564 - 0.1846154 Total gas flow(sccm)

Figure 39. Effect of the total gas flow

barely around 40%. Therefore, the total gas flow has to be fixed between 250 sccm and 300 sccm.

Figure 40 shows the effect of C_4F_8/O_2 gas ratio. The selectivity of oxide over TiN can reach to 28:1 when the gas ratio is about 2.25. However, the etch stop is found in the center of the wafer. Both selectivity and etch depth are decreased with the higher gas ratio. Therefore, reasonable selectivity and enough etch depth can be obtained when the gas ratio is around 2.

4.3.2 Second DOE

The key parameters for the regular via etching process are pressure, C_4F_8 gas flow, and O_2 gas flow. It is based on the first DOE after the chuck temperature is fixed at 40 °C for both contact and via etching processes.

The variation ranges of the key parameters for the second DOE are:

Pressure: 40 mT to 50 mT

C_4F_8 gas flow: 8 sccm to 12 sccm

O_2 gas flow: 5 sccm to 7 sccm

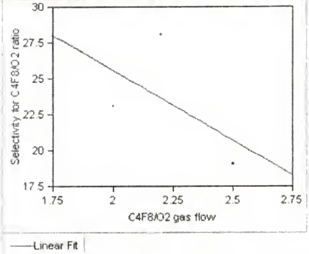
The responses are etch depth, etch stop, TiN loss, top CD, and PR remaining. Nominal and subnominal sections have been investigated. Section 5 is the nominal area, and section 4 is the subnominal area.

Table 3 presents the design plan of the second DOE. There are 10 VIAZT wafers that are etched by following the variety parameters.

The cross-section SEM pictures have been completed on the Hitachi-4500 for the 10 wafers. The pictures are taken on both the center and edge of the wafers.

Figure 41 shows the process trend of etch depth associated with the different

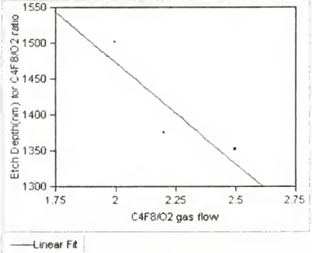
Bivariate Fit of Selectivity for C4F8/O2 ratio By C4F8/O2 gas flow



Linear Fit

Selectivity for C4F8/O2 ratio = 45.078947 - 9.7368421 C4F8/O2 gas flow

Bivariate Fit of Etch Depth(nm) for C4F8/O2 ratio By C4F8/O2 gas flow



Linear Fit

Etch Depth(nm) for C4F8/O2 ratio = 2039.2105 - 282.63158 C4F8/O2 gas flow

Figure 40. Effect of C_4F_8/O_2 gas ratio

Table 3 - Design plan for the second DOE

	pattern	pressure(mT)	C_4F_8(sccm)	O_2(sccm)
run1	++-	50	12	5
run2	--+	40	8	7
run3	0	45	10	6
run4	-++	40	12	7
run5	+++	50	12	7
run6	+-+	50	8	7
run7	+--	50	8	5
run8	---	40	8	5
run9	-+-	40	12	5
run10	0	45	10	6

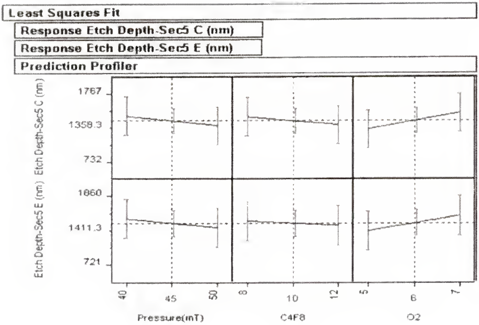


Figure 41. Etch depth at nominal section
(Note: top – center of the wafer, bottom – edge of the wafer)

parameters at nominal section. The trend on the center and edge of the wafers is very consistent as pressure, C_4F_8 and O_2 gas flows change. There is no significant change for the etch depth when pressure and C_4F_8 gas flow change. However, the etch depth varies sensitively when the O_2 gas flow changes. Therefore, two VIAZT lots are split by varying O_2 gas flow when we check over-etch process margin. The split cells are: 5 sccm, 5.5 sccm, 6 sccm, 6.5 sccm, 7 sccm, and 7.5 sccm O_2 gas flow when other parameters are fixed at the baseline points. The variation trend of the electrical data is collected on these split lots. The center point of O_2 gas flow is optimized after these two split lots are completed. In addition, the process trend can be predicted accurately from Figure 41 when O_2 gas flow varies. This is the biggest advantage to use JMP software to analysis the DOE results. For example, the exact etch depth as the O_2 gas flow changes can be read out when the cursor is in the any points between 5 sccm and 7 sccm O_2. This means that it is not necessary to etch the actual wafer to check the etch depth if the O_2 gas flow is needed to be 5.5 sccm. This is the reason why the JMP software is so popular in the semiconductor industry.

Figure 42 shows the etch stop is observed at nominal section when the etching parameters vary. It also can predict the possibility of etch stop for the different setting points in x axis. The etch stop is observed from the etch front of the cross-section SEM pictures. In Figure 42, “1” represents without etch stop, and “2” represents etch stop. The results in Figure 42 indicate that C_4F_8 and O_2 gas flows do not affect the trend of etch stop. On the other hand, pressure plays a very important role for the trend of etch stop. The higher pressure, the more possibility to have the etch stop.

Figure 43 shows the TiN loss at nominal section as the three etching parameters

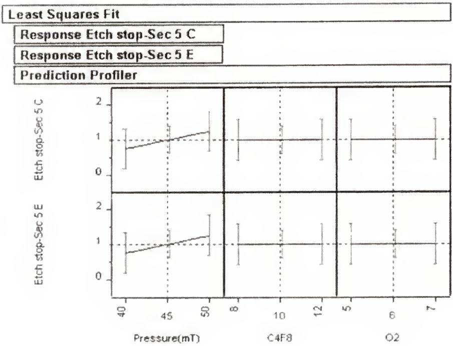


Figure 42. Etch stop at nominal section
(Note: top – center of the wafer, bottom – edge of the wafer)

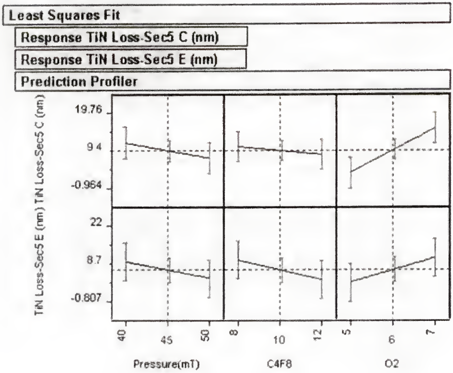


Figure 43. Loss of TiN at nominal section
(Note: top – center of the wafer, bottom – edge of the wafer)

change. O_2 gas flow affects the TiN loss dominantly. This means more TiN loss with higher O_2 gas flow. Therefore, more careful research work needs to be finished for the small O_2 gas flow change. Higher pressure and more C_4F_8 gas flow are probably helpful to have less TiN loss.

Figure 44 shows the trend of the top CD at the nominal section as the etching parameters change. The variation of pressure affects the top CD primarily. The lower pressure can make the top CD be smaller. Therefore, lower pressure etch equipments are very popular for the submicron technologies. The top CDs are very consistent on the center and edge of the wafer. It indicates that the uniformity of the top CD is not sensitive to the variation of these three major etching parameters.

Figure 45 shows the trend of PR remaining at the nominal section as the etching parameters change. It indicates that the O_2 gas flow is the key parameter to control PR remaining. The more O_2 gas flow, the less PR remaining. It can be explained by the basic reaction theory applied for the PR strip process. The volatile products of CO or CO_2 are produced when the organic material — PR is reacted with O_2 gas. Then CO or CO_2 can be pumped away from the chamber. Therefore, less O_2 gas flow needs to be added if the thickness of PR is very marginal for the advanced technologies.

Figure 46 shows the trend of etch depth at the subnominal section. The data on subnominal section is very important to develop the novel technologies with much smaller feature size in the future. More O_2 gas flow is more helpful to have the over-etch margin at the subnominal section based on the trend curves. However, the PR remaining margin drops significantly with more O_2 gas flow as mentioned previously. The etching process has to be trade-off between the PR remaining and over-etch margin.

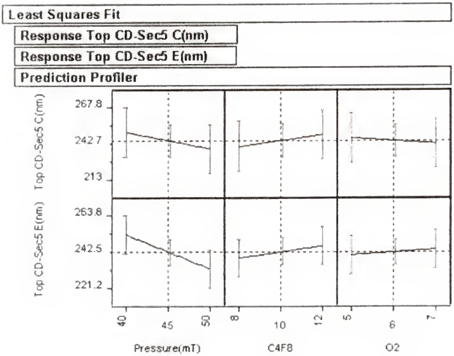


Figure 44. Top CD at nominal section
(Note: top – center of the wafer, bottom – edge of the wafer)

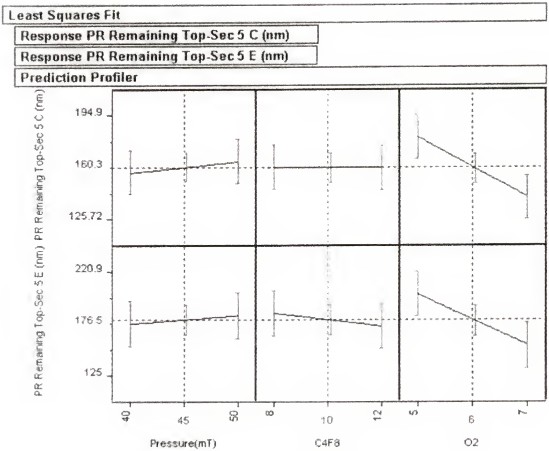


Figure 45. Remaining Photo-Resist (PR) at nominal section
(Note: top – center of the wafer, bottom – edge of the wafer)

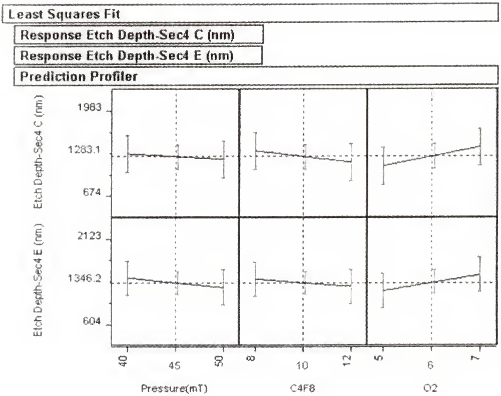


Figure 46. Etch depth at subnominal section
(Note: top – center of the wafer, bottom – edge of the wafer)

Figure 47 shows the trend of the etch stop at subnominal section when the parameters vary. More C_4F_8 and less O_2 gas flows can cause more possibility to have the etch stop. Pressure does not affect the trend of the etch stop.

Figure 48 shows the variation trend of the top CD at subnominal section when the etching parameters change. The top CD on the edge of the wafer is increased when the O_2 gas flow is increased. However, the range of the top CD at subnominal section is only ±0.003 μm that is very small amount of CD bias before and after etching. Therefore, the uniformity of top CD between center and edge of the wafer is reasonable to be accepted by using the center point process.

In summary, the current baseline recipe can provide enough over-etch margin, PR remaining margin, tight CD control, reasonable TiN loss on the nominal sections based on the results of the DOE.

4.4 Final Recipe

4.4.1 Process Margin Improvement

The baseline process can deliver acceptable products. However, it is very marginal at the subnominal sections. It means that the electrical data is not consistent from lot to lot at the subnominal sections. We found out the issue is relative to the small over-etch margin at the subnominal sections.

The O_2 gas flow is very critical to control the over-etch margin from the above DOE results. Therefore, one more sccm O_2 is added to the Main etching step in order to improve over-etch margin at the subnominal sections and still can maintain similar CD bias and reasonable PR remaining. Figure 49 shows the cross-section SEM pictures at the subnominal sections by applying the baseline and new recipes. The etch depth is very similar either on the center or on the edge of the wafers. However, the significant

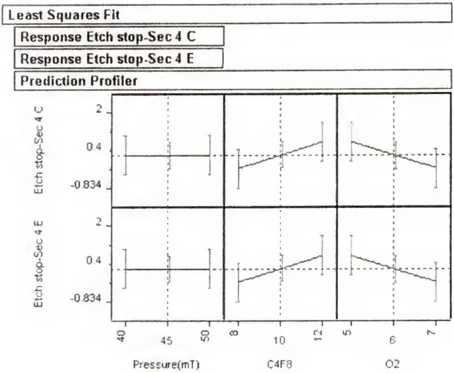


Figure 47. Etch stop at subnominal section
(Note: top – center of the wafer, bottom – edge of the wafer)

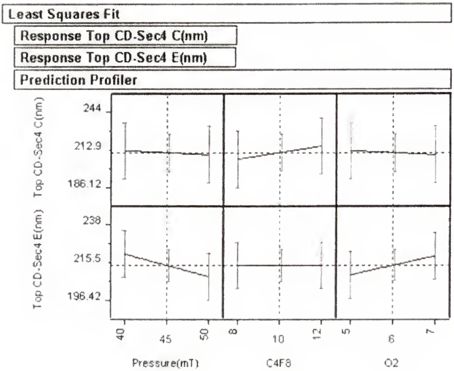


Figure 48. Top CD at subnominal section
(Note: top – center of the wafer, bottom – edge of the wafer)

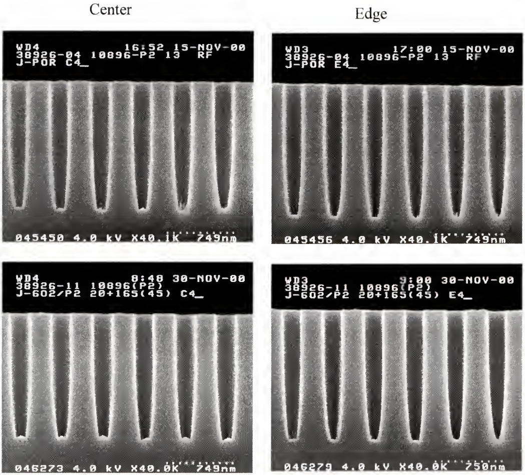


Figure 49. Cross-section SEM pictures for baseline and new recipes
(Note: top – baseline recipe for center and edge of the wafer, bottom – new recipe for center and edge of the wafer.)

difference can be observed when we add 20% more over-etch time based on the experiments shown in Figure 49. Figure 50 shows the results clearly. The etch stop happened when 20% more over-etch time is added to the baseline recipe. Oppositely, the expected over-etch depth without etch stop is obtained when 20% more over-etch time is added to the new recipe. The following work is to evaluate the effect of the new process on the electrical data output. Finally, much better electrical data is obtained at the subnominal sections by using the new process and the comparable electrical data is also obtained at the nominal sections from several split lots. Therefore, this modified recipe is implemented inline to be the new POR for via etching process.

4.4.2 Top-down Scanning Electron Microscope (SEM)

More evaluation work needs to be completed after the final recipe is fixed. The top-down CD SEM pictures are taken before via etching, after PR strip, after wet clean, and after dry clean in order to monitor the inline CD bias without cleaving the wafers. Figure 51 shows the top-down CD SEM pictures before via etching process. It is the reference to monitor the CD variation after etching.

Figure 52 shows the top-down CD SEM pictures and CD bias after via etching and PR strip. The CD bias is around 0.01 μm after PR strip. The top-down CD SEMs are very similar between before via etching and after PR strip. In addition, the bottom of the vias is very clean after PR strip and it indicates that there is no descum is caused by the via etching process. In another word, main etching is stopped on the TiN layer smoothly and successfully.

Figure 53 shows the top-down CD SEM pictures after wet clean. The purpose of the clean step is to take the by-products and polymers deposited on the sidewall and

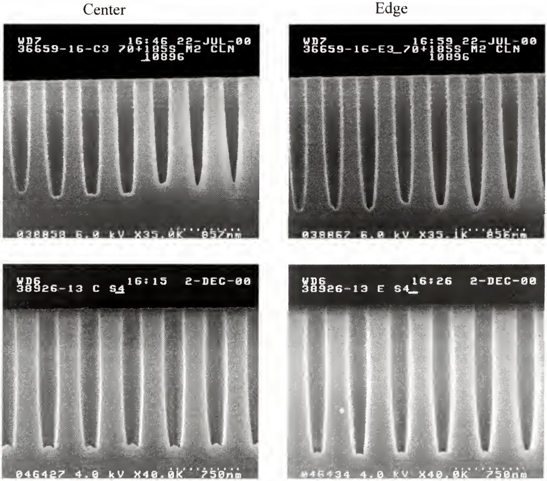
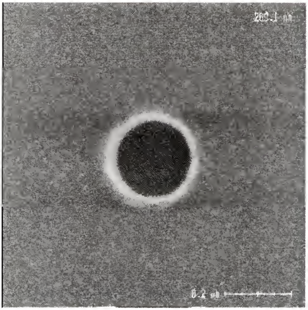

Center
Edge
WD7 16:46 22-JUL-00
36659-16-C3 70+185S M2 CLN
10896
038858 6.0 kV X35.0K 857nm
WD7 16:59 22-JUL-00
36659-16-E3_70+185S M2 CLN
10896
038867 6.0 kV X35.1K 856nm
WD6 16:15 2-DEC-00
38926-13 C S4
046427 4.0 kV X40.0K 750nm
WD6 16:26 2-DEC-00
38926-13 E S4
046434 4.0 kV X40.0K 750nm

Figure 50. Cross-section SEM pictures for baseline and new recipes with more 20% over etching time
(Note: top – baseline recipe for center and edge of the wafer, bottom – new recipe for center and edge of the wafer.)

Center



Edge

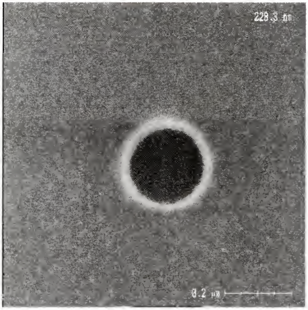
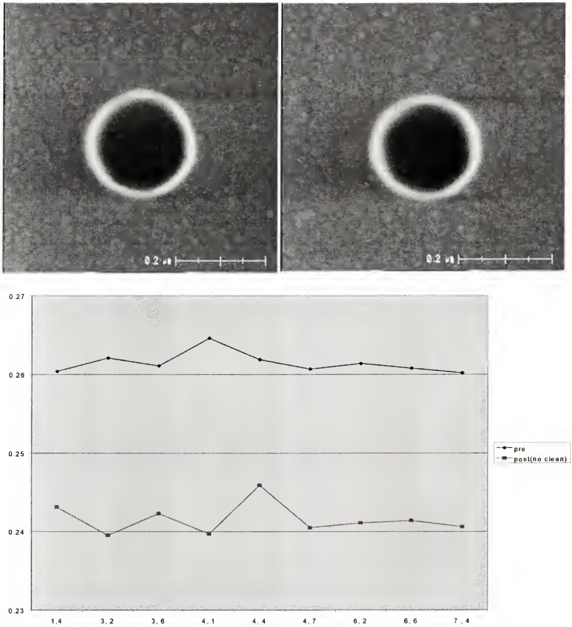


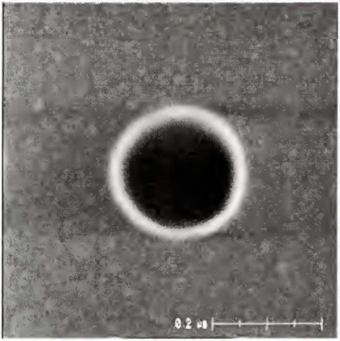
Figure 51. Top-down CD SEM pictures before via etching


Center

Edge

Figure 52. Top-down CD SEM pictures and CD bias after PR strip

Center



Edge

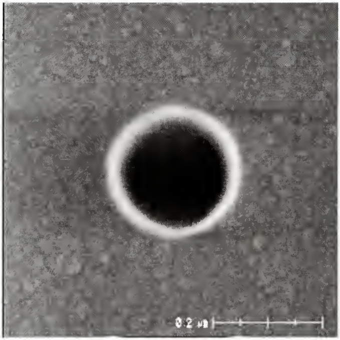


Figure 53. Top-down CD SEM pictures after wet clean

bottom of the vias after via etching. Again, there is no descum on the bottom of the vias. It is very similar with the pictures in Figure 52.

Figure 54 shows the top-down CD SEM pictures and the cross-section SEM pictures after dry clean. The small amount of descum is shown on the bottom of the vias on both center and edge of the wafer. It indicates that the dry clean step not only takes away the polymers on the bottom of vias but also etches away some amount of TiN layer. It causes the undercutting shown in the cross-section SEMs obviously. Therefore, the clean engineer has to develop a new process to reduce the undercutting on the bottom of vias. The drawback of the undercutting is that the contact resistance can be affected after W plugs deposited in the vias. Please note that the same wafer is used from Figure 51 to Figure 54.

4.4.3 Stability of the Final Process

The repeatability of the final process has to be checked before it is delivered to the production lines completely. There are two aspects to test the repeatability of the process:

- The consistency from wafer to wafer. The method is to put the VIAZT wafers in the slots 1 and 25. The blanket Photo-Resist wafers are put between slots 2 and 24. The whole lot is etched by using the final recipe. The two VIAZT wafers are PR stripped in the same chamber after via etching. Then the cross-sections are done on these two wafers. Figure 55 shows the cross-section SEM pictures after the above experiment. The via profiles are very similar between slots 1 and 24. It demonstrates that the final process is repeatable from wafer to wafer within the lot.

- The consistency from lot to lot. The method is to compare the cross-section SEM pictures from the wafers etched within the different RF hours. Usually, the wet clean on the chamber needs to be done after 100 RF hours for dielectric etching chamber. RF hours is reset to zero after the wet clean. Therefore, three wafers can be etched in the beginning, middle, and end of this cycle period. Figure 56 shows the cross-section SEM pictures for one cycle period. The results are similar among these different timeframe. This also indicates the final process is repeatable and

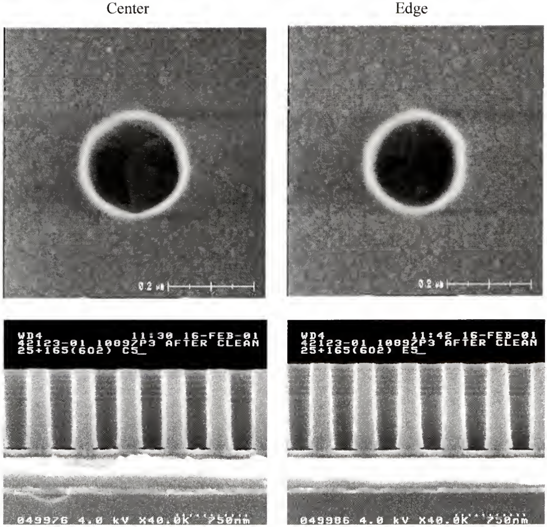

Center
Edge
0.2 µm
0.2 µm
WD4 11:30 16-FEB-01
42123-01 10097P3 AFTER CLEAN
25+165(602) C5_
WD4 11:42 16-FEB-01
42123-01 10097P3 AFTER CLEAN
25+165(602) E5_
049976 4.0 kV X40.0K 750nm
049986 4.0 kV X40.0K 750nm

Figure 54. Top-down CD and cross-section SEM pictures after wet clean

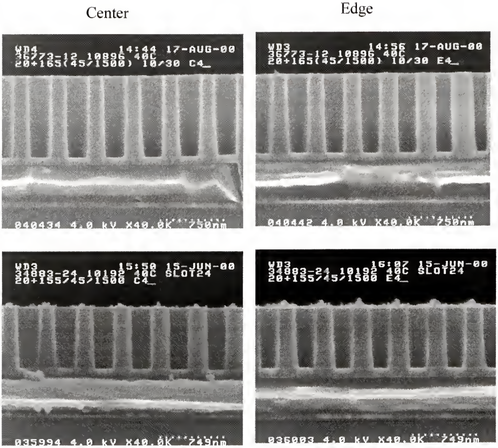

Center
Edge
WD4 14:44 17-AUG-00
36773-12 10896 40C
20+165(45/1500) 10/30 C4_
040434 4.0 kV X40.0K 750nm
WD3 14:56 17-AUG-00
36773-12 10896 40C
20+165(45/1500) 10/30 E4_
040442 4.0 kV X40.0K 750nm
WD3 15:50 15-JUN-00
34883-24 10192 40C SLOT24
20+155/45/1500 C4_
035994 4.0 kV X40.0K 749nm
WD3 16:07 15-JUN-00
34883-24 10192 40C SLOT24
20+155/45/1500 E4_
036003 4.0 kV X40.0K 749nm

Figure 55. Cross-section SEM pictures of the wafers in slots 1 and 24
(Note: top – slot 1, bottom – slot 24.)

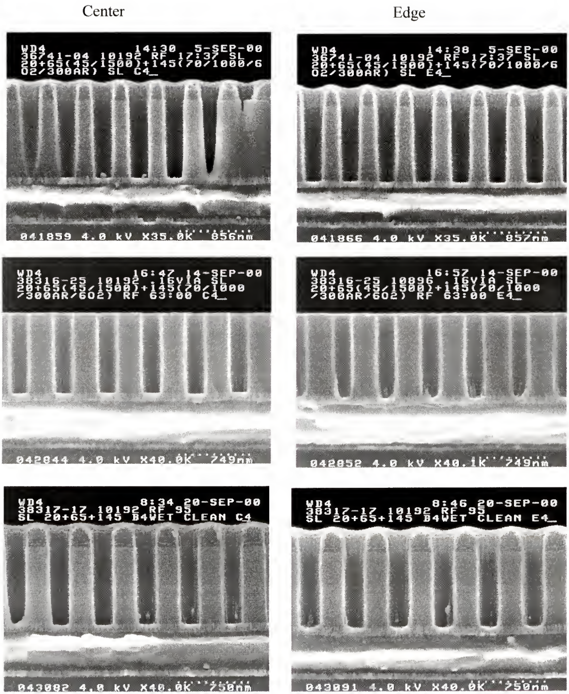


Figure 56. Cross-section SEM pictures for one cycle period
(Note: top – RF hours: 17:37, middle – RF hours: 63:00, bottom – RF hours: 95:00.)

manufacturable. On the other hand, the above data demonstrated the medium-density plasma etcher is a reliable tool for the high volume manufacture demand.

The electrical data is also collected to verify the stability of the final process on 30 to 50 lots. Plus, the gate leakage data is collected on several lots in order to check the effect of PID from the medium-density plasma etcher. The final electrical data indicates the damage is caused by the modified via etching process on the medium-density plasma etcher is acceptable. Finally, the robust via etching process is delivered to the product lines after the comparable electrical data is obtained on those lots.

CHAPTER 5
ETCHING PROCESS FOR TAPERED VIAS

5.1 Introduction

This special etching process is only developed for the analog circuits. The Tungsten (W) seams are exposed on the top of the vias that caused the metal filling in the seam that strongly affects the deposition of the above thin oxide layer. The tapered via is very helpful to lower down the seams or voids when W plugs deposited. The contact resistance can be reduced and yield can be improved significantly by applying this irregular via etching process. Figure 57 shows the structures with and without the tapered via. The biggest challenge is to taper the top of the vias and maintain the straight profile on the bottom of vias, meanwhile to have enough Photo-Resist margin to avoid the overlapping of neighboring vias. Tapered oxide depth is asked for less than 1000 Å.

The Ex-situ and In-situ processes were evaluated together. The idea of Ex-situ process is to get the straight via done first and strip the Photo-Resist, and come back to etch again on the same etching chamber to round the corner of the vias. This means the surface of the oxide layer is totally exposed to the plasma without Photo-Resist. The advantage of this process is that it is very easy to control the taper angle of the round corner during Round Corner (RC) step. The In-situ process is more complicated compared with the Ex-situ process since it needs to round the corner and have the straight via bottom within only one etch step. However it can reduce the cycle time and cost of ownership.

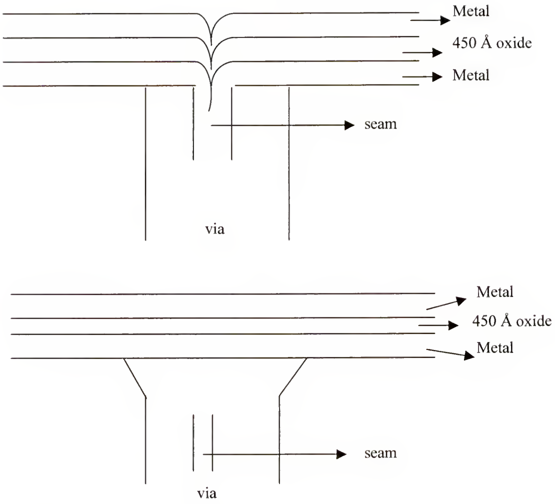


Figure 57. Structures with and without the tapered vias
(Note: top – without tapered vias, bottom – with tapered vias.)

5.2 Development of Process

5.2.1 Ex-Situ process

Originally, the concept of the tapered via needs to be verified on the cross-section SEM pictures after W plugs are deposited. The Ex-situ process is developed first because it is easier to develop inline. The method of Ex-situ process is to finish the main etch and have the via profile, and PR strip the wafer, and etch the wafer again in a short time in order to etch away the exposed oxide in the corner of vias. The key issue to develop this process is to control the etch time of the last etch step. It is also called "Round Corner (RC)" step. The goal of RC step is to round the corner of vias and maintain the oxide thickness in the gap between the neighboring vias as much as possible. The neighboring vias are overlapped if the top of vias is opened too widely. Then the overlapped vias can cause the failure of the devices. Therefore, one optimized process needs to be developed to meet the above requirements.

There are two approaches to maintain enough oxide thickness between the neighboring vias: one is to increase the oxide thickness before photolithography step and another one is to develop a gentle RC process. For the first approach, it is very necessary to consider more over-etch during main etch step since the incoming wafers has 1000 Å more oxide thickness. For the second approach, it is hard to have the required oxide thickness for the round area if we develop the gentle RC process. Therefore, the research work is focused on the first approach only because it is easier to control the process. The baseline recipe is to use the same etching condition in the RC step as the main etch step and shorter the etch time to 35 seconds. Figure 58 shows the cross-section SEM pictures for this baseline process. The process flow of the baseline process is: SPARC etch + Main etching on the etching tool, PR strip on Gasonic tool (San Jose, CA, USA), and RC

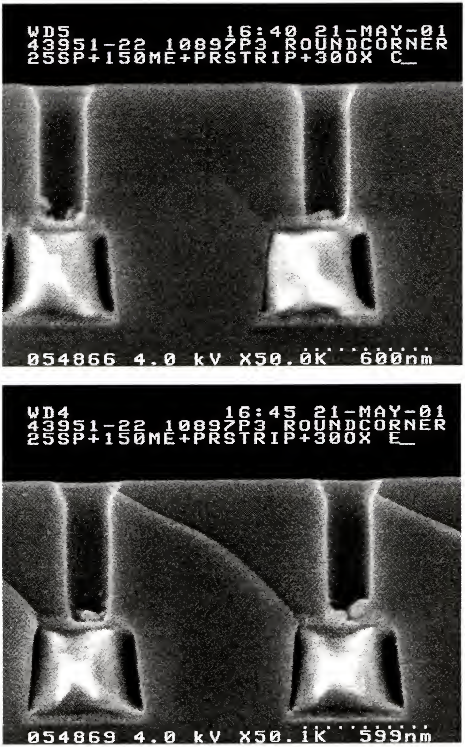
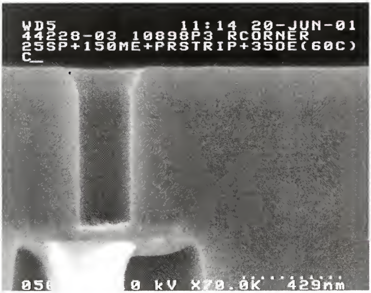

WD5 16:40 21-MAY-01
43951-22 10897P3 ROUNDCORNER
25SP+150ME+PRSTRIP+300X C_
054866 4.0 kV X50.0K 600nm
WD4 16:45 21-MAY-01
43951-22 10897P3 ROUNDCORNER
25SP+150ME+PRSTRIP+300X E_
054869 4.0 kV X50.1K 599nm

Figure 58. Cross-section SEM pictures for the baseline process
(Note: top – center of the wafer, bottom – edge of the wafer.)

etching on the etching tool again. The TiN gauging is around 300 Å and is not acceptable by the integration requirement. In addition, there are some polymers deposited on the bottom of vias. They cannot be taken away after the wet and dry clean processes. These uncleaned polymers affect the electrical results tremendously. Therefore, another modified process has to be developed to have less TiN gauging. There are two options to meet this requirement. One is to raise the chuck temperature to have higher selectivity of oxide over TiN, and another one is to reduce the He backside pressure to increase the selectivity of oxide over TiN. The first option has the similar drawback as we mentioned in Chapter 4 for the regular via etching process. The chuck temperature has to be raised before RC step every time. It is not manufacturable and acceptable. However, the experiment needs to be executed to verify the concept. The process flow of Option 1 is: SPARC etch + Main etching on the etching tool, PR strip on Gasonic tool, and RC etching (chuck temperature: 60 °C) on the etching tool again. Figure 59 shows the cross-section SEM pictures for higher chuck temperature RC process. The differences between the Option 1 process and the baseline process are the chuck temperature and etch time. The etch time of Option 1 has been increased in order to compensate the similar amount of over-etch. The TiN gauging is decreased to 200 Å dramatically, and the thickness of the rounded oxide depth is around 1070 Å as required. The good uniformity is obtained during this process. Therefore, we continued to develop the Option 2 process based on the same assumption. In fact, the chuck temperature is increased when the He backside pressure is decreased. It means that the effect of the Option 2 is very similar with the Option 1. The biggest advantage of the Option 2 is that the chuck temperature does not need to increase to 60 °C before RC etching. Figure 60 shows the cross-section SEM

Center



Edge

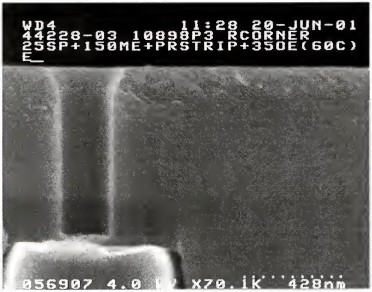
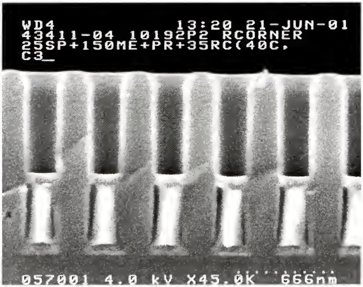


Figure 59. Cross-section SEM pictures for Option 1
(Note: top – center of the wafer, bottom – edge of the wafer.)

Center



Edge

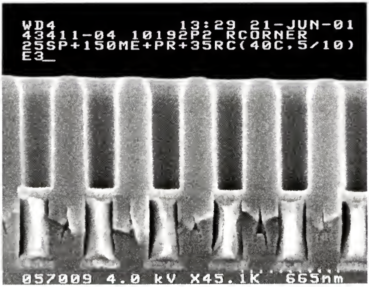


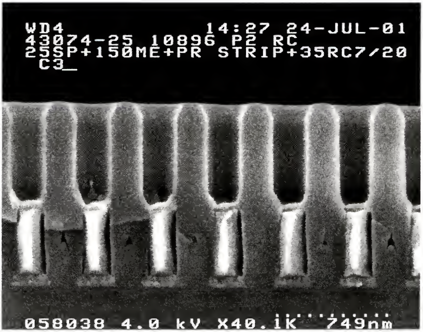
Figure 60. Cross-section SEM pictures for Option 2
(Note: top – center of the wafer, bottom – edge of the wafer.)

pictures for Option 2. The TiN gauging is very close to the TiN gauging of Option 1 and is also around 200 Å. The thickness of the rounded oxide area is about 1100 Å after RC etching. The integration engineers are very satisfied with the results. The electrical data for Option 1 and Option 2 are very comparable based on several split lots. Then the near future work is narrowed down to adjust the He backside pressure to check the process margin. Therefore, the VIAZT wafers are used to test the processes at much lower and much higher He backside pressures. The process at much lower He backside pressure shows the best electrical results among the split cells. Figure 61 shows the cross-section SEM pictures of the process at higher He backside pressure. Figure 62 shows the cross-section SEM pictures of the process at lower He backside pressure. Finally, the process at lower He backside pressure is implemented inline for the product of analog circuits. The TiN gauging is about 180 to 190 Å; 30 to 40% over-etch is obtained at the subnominal section and 40 to 50% over-etch is obtained at the nominal section; the oxide thickness of the rounded area is around 990 Å; and the distance between the neighboring vias is around 1000 Å. Figure 63 shows the cross-section SEM pictures at lower He backside pressure after W plugs deposited. It indicates that the corner of vias has been rounded and the seam has been lowered down to the middle of the vias.

5.2.2 In-Situ Process

The In-situ processes for 0.25 μm and bigger technologies have been developed and implemented in the product lines successfully. The purpose of the In-situ process is to create the round corner and etch via profile in the same etching step. It can reduce the cycle time extremely since only one tool is involved during the process. In addition, the etch process is much more simple than the Ex-situ process. However, the disadvantage of

Center



Edge

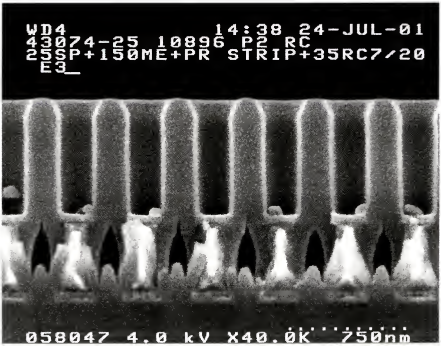
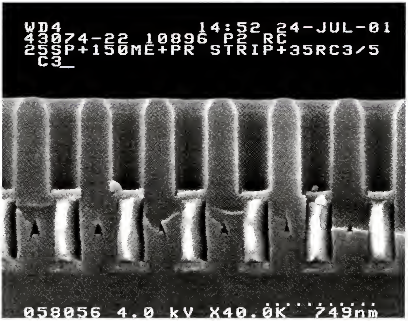


Figure 61. Cross-section SEM pictures for higher He backside pressure
(Note: top – center of the wafer, bottom – edge of the wafer.)

Center



Edge

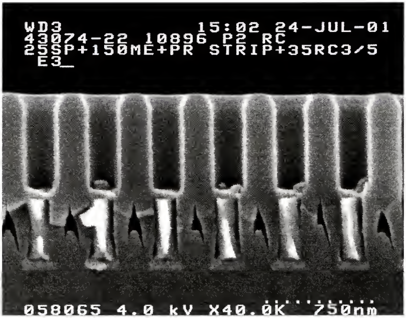


Figure 62. Cross-section SEM pictures for lower He backside pressure (Note: top – center of the wafer, bottom – edge of the wafer.)

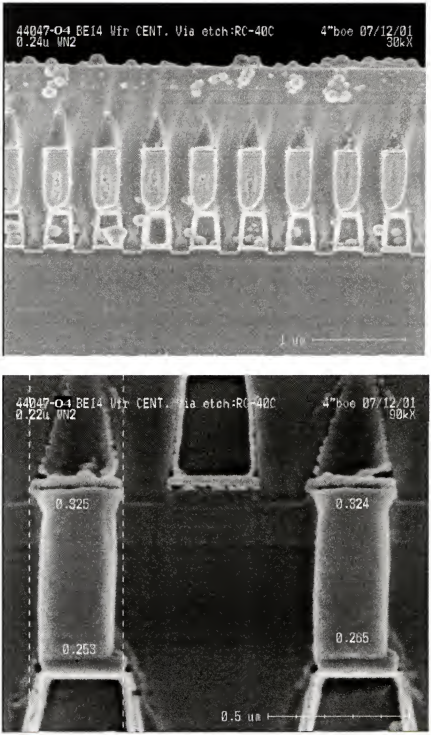
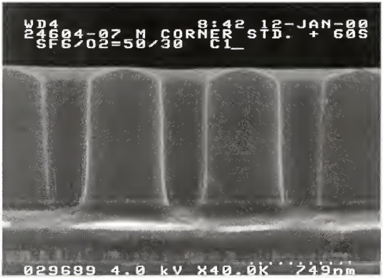


Figure 63. Cross-section SEM pictures for lower He backside pressure after W plugs deposited
(Note: top – smaller magnification, bottom – higher magnification.)

the In-situ process is that it takes much longer time to develop the process due to much more cross-section work. At first, the selectivity of oxide over PR has to be obtained by using the mechanical oxide and PR wafers. The ideal selectivity should be around 1:1 which means that it is easier to expose the corner of vias to plasma. Meanwhile, the gap between the neighboring vias can be protected by Photo-Resist very well to avoid overlapping. The via etching process for 0.25 μm and bigger technologies is to breakthrough the TiN layer instead of stopping on the TiN layer. The first etching chemistry used for this application is SF_6. Figure 64 shows the cross-section SEM pictures for SF_6 In-situ process. The corner of vias is rounded as required. However, too much oxide loss in the area between the neighboring vias that causes the connections of vias. It indicates that the high selectivity of PR over oxide causes too much PR is etched away when the corner of vias is rounded. Therefore, SF_6 is too aggressive for PR consumption during RC step. Secondly, an O_2 flash step is used to etch away PR around the corner before RC step in order to expose the oxide in the corner. Figure 65 shows the cross-section SEM pictures for O_2 flash process. This is even worse than the SF_6 process since more overlapped vias are observed. Finally, O_2 is added to the TiN breakthrough step with CF_4/Ar together to finish TiN breakthrough and round corner in the same step. The percentage of O_2 flow is studied by using the mechanical wafers in order to have 1:1 selectivity of PR over oxide. Figure 66 shows the relationship between the percentage of O_2 flow and selectivity of PR over oxide. It is easy to find how many percentage of O_2 is added if the selectivity of PR/oxide is 1:1. Figure 67 shows the cross-section SEM pictures for this novel process. More PR is preserved in the area between neighboring vias during RC step. Figure 68 shows the cross-section SEM pictures for this new process

Center



Edge

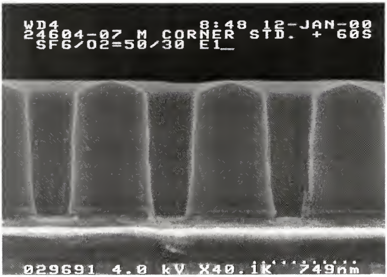
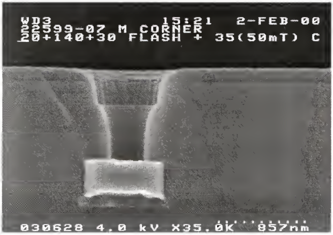
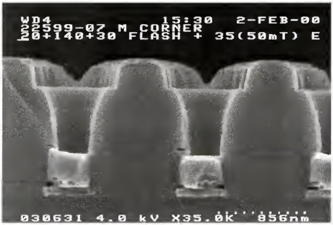


Figure 64. Cross-section SEM pictures for SF_6 Round Corner (RC) process (Note: top – center of the wafer, bottom – edge of the wafer.)

Center



Edge



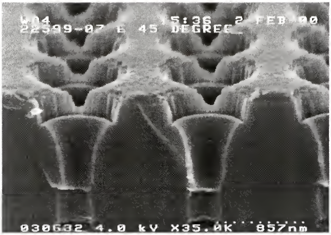


Figure 65. Cross-section SEM pictures for O_2 flash RC process
(Note: top – center of the wafer, middle – edge of the wafer, bottom – top down.)

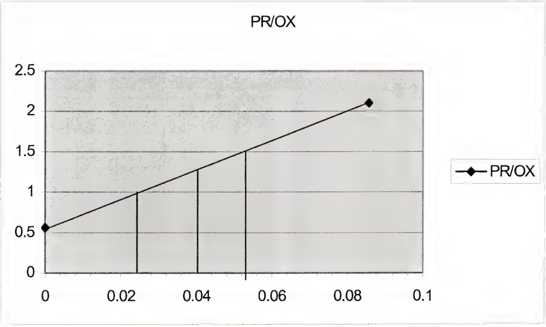
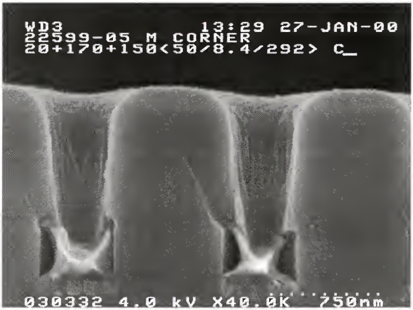


Figure 66. Percentage of O_2 flow vs selectivity of PR over oxide

after W plugs are deposited. The seam is lowered down obviously and the round corner of vias can be seen clearly. The new In-situ process allows a better W filling and pushes down the W seams in via plug with maintaining the straight profile of the bottom of vias. It combines TiN breakthrough process and round corner process to only one step by introducing new gas — O_2 and adjusting the gas ratio of $CF_4/O_2/Ar$. It preserves more PR on the top of the space between the vias to avoid overlapping vias, and significantly simplified and optimized the etch process, and greatly shorten the cycle time to save more money. In addition, the margin of the etch process is also increased. The yield of the products is 15% higher and the contact resistance is 17% lower than non-tapered via process.

The In-situ process for stopping on TiN (0.18 μm and below technologies) is still developing due to its complication. There are some PR remaining on the corner of the vias and the corner is still straight when we use the In-situ process of 0.25 μm technology. Therefore, we use a new gas combination of $CHF_3/CO/O_2$ to continue to develop the In-situ process. The etch stop shows up for this new combination. Figure 69 shows the cross-section SEM pictures for both of the cases. In the future, more development work needs to be done to find a better etching chemistry that has higher etch rate on Photo-Resist in order to expose the corner of vias that is rounded eventually.

Center



Edge

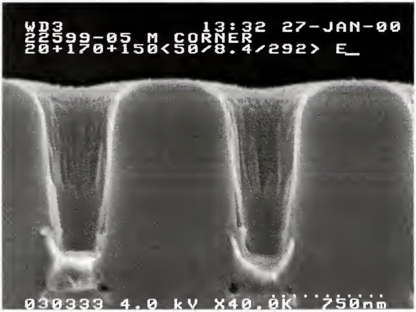
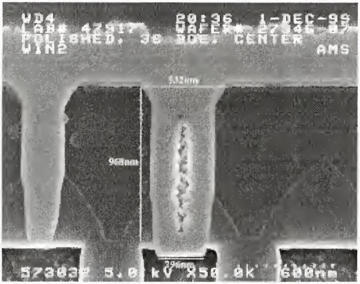


Figure 67. Cross-section SEM pictures for new RC process
(Note: top – center of the wafer, bottom – edge of the wafer.)

Center



Edge

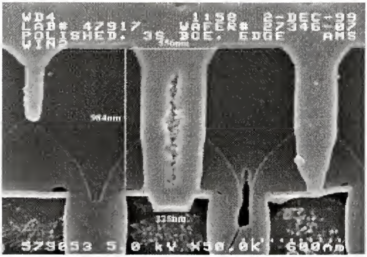

WD4 1:58 2-DEC-99
LAB# 47917 WAFER# 27346-07
POLISHED. 3S BOE. EDGE AMS
WIN2
556nm
984nm
335nm
579653 5.0 kV X50.0k 600nm

Figure 68. Cross-section SEM pictures for new RC process after W plugs deposited (Note: top – center of the wafer, bottom – edge of the wafer.)

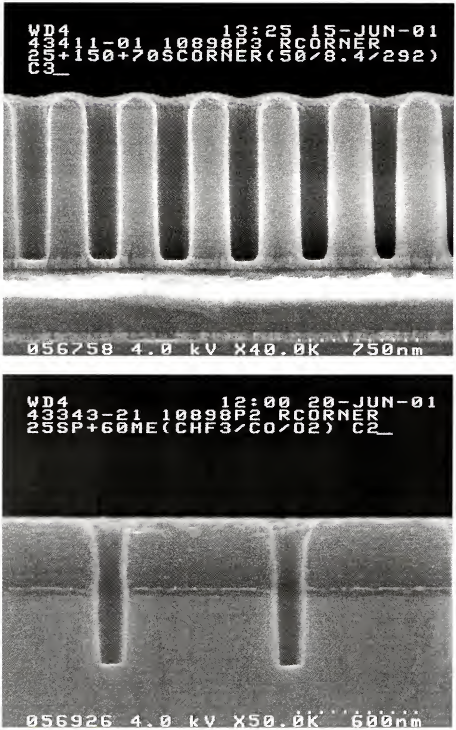

WD4 13:25 15-JUN-01
43411-01 10898P3 RCORNER
25+150+70SCORNER(50/8.4/292)
C3_
056758 4.0 kV X40.0K 750nm
WD4 12:00 20-JUN-01
43343-21 10898P2 RCORNER
25SP+60ME(CHF3/CO/O2) C2_
056926 4.0 kV X50.0K 600nm

Figure 69. Cross-section SEM pictures for In-situ processes on the center of wafers (Note: top – 0.25 μm RC process, bottom – gas combination of $CHF_3/CO/O_2$.)

CHAPTER 6
ETCHING PROCESS FOR SELF-ALIGNED CONTACT (SAC)

6.1 Introduction

The Self-aligned Contact (SAC) etching process is only for Embedded SRAM (ESRAM) circuits. The process flow for SAC etching process is: SAC etching, SiN layer break-through, and standard contact etching. It consists of two photolithography and three etching processes. Most of the following discussion is focused on the SAC etching process only. High selectivity to SiN in SiO_2 etching is crucial to realizing high-performance and low-cost semiconductor devices so that it is possible to form self-aligned and borderless contact hole structure.[33-36]Compared with the regular contact etching process, SAC etching process is more challengable because the selectivity of oxide/SiN must be higher than 20:1. A SiO_2/SiN selective etching is more difficult than a SiO_2/Si one, because the etching characteristics of SiN are similar to those of SiO_2.[33, 36-41] We need to consider two steps etching process to balance oxide over-etch margin and higher selectivity of oxide/SiN. The purpose of the first etch step is to have the higher etch rate in order to guarantee enough over-etch for the thick oxide layer. The second etch step has slower etch rate but higher selectivity of oxide/SiN to avoid less SiN gauging. It is designed to be a “soft” etch process. Many studies have reported that C_4F_8 is effective in reducing the amount of F, which etches SiN. But high selectivity was achieved only when CO was added to C_4F_8 in magnetron plasma, the role of CO is to scavenge fluorine by forming COF_x. Thus the reliable, highly selective SiO_2 etching process over SiN with C_4F_8 + CO magnetron plasma is established. Figure 70 shows the

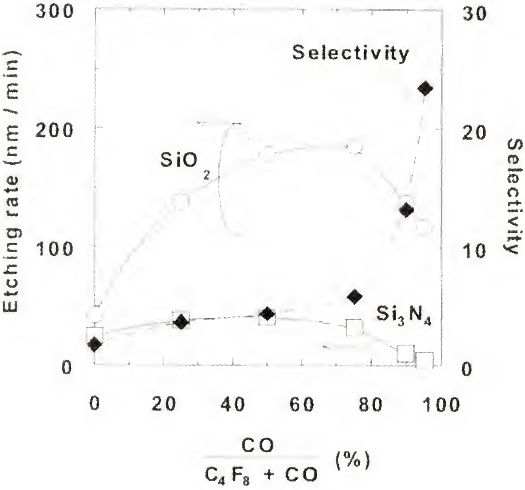


Figure 70. SiO_2 and SiN etching rates as a function of CO flow rate ratio, together with the corresponding selectivity between SiO_2 and SiN etching rates

SiO_2 and SiN etching rates as a function of the CO flow rate ratio. The selectivity between SiO_2 and SiN etching rates is also shown. The SiO_2 etching rate increased up to the CO ratio of 75% and dropped afterwards. Because the excess fluorocarbon radicals in C_4F_8 plasma, such as CF, formed a thick fluorocarbon film on the SiO_2 surface and obstructed the progress of the etching. The density of the fluorocarbon radicals is decreased due to diluting effects when CO is added to C_4F_8 gas. Therefore, the etching rate of SiO_2 is increased. On the other hand, the etching rate of SiO_2 is decreased when the CO ratio is more than 75% because of the lack of etchants, such as fluorine and CF_2 radical, which enhance the SiO_2 etching with ion bombardment. The SiN etching rate exhibited the same tendency as the SiO_2 etching rate.[41-52] In order to increase SAC process margin, different etch tools, various gases are studied extensively. Two high-density plasma tools are evaluated with the medium-density plasma tool together. The high-density plasma tool can provide higher selectivity of oxide/SiN than the current medium-density plasma etcher. The novel gases- C_5F_8 and C_4F_6 also are investigated on the high-density plasma tools.

6.2 Development of Process

6.2.1 Baseline Recipe

Figure 71 shows the film stacks of the SAC. The oxide layers are very similar to the film stacks of the regular contact. However, there is one thin SiN layer between the oxide layer and Si and it needs to be etched through. Therefore, the process flow is: SAC etching that stops on the SiN layer, SiN etching, photolithography and standard contact etching. The baseline SAC recipe was developed on the medium-density plasma etcher for 0.20 μm technology. Figure 72 shows the cross-section SEM pictures for the baseline SAC process. SAC etching stops on the SiN layer successfully and there are

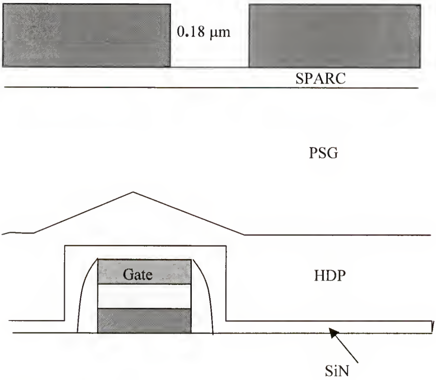
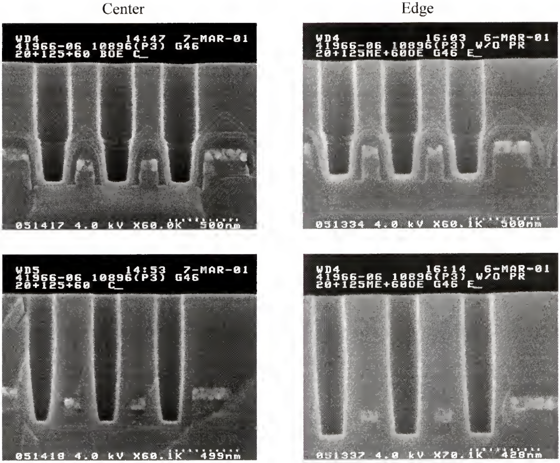


Figure 71. Film stacks for SAC


Center

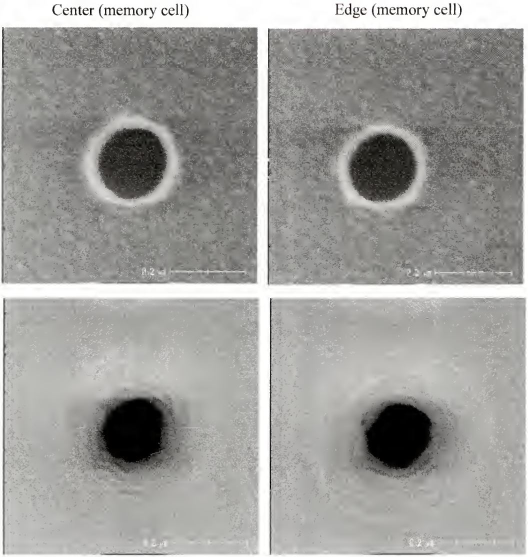
Edge

Figure 72. Cross-section SEM pictures for the baseline SAC etching process (Note: top - with 3 seconds BOE treatments, bottom – without BOE treatment.)

enough SiN remaining on the corner of the SiN layer that can protect the gate area effectively. It demonstrates that good selectivity of oxide over SiN is obtained for this technology. The contact profile has been shaped as required. The etched wafer is treated by 3 seconds BOE in order to see the interface between oxide layer and SiN layer clearly. Please notice that the final CD is always bigger after the BOE treatment. Therefore, the profile of the SAC is only based on the cross-section SEM pictures without the BOE treatment. Figure 73 shows the top-down CD SEM pictures before and after SAC etching inside the memory cells. The top-down SEMs are very consistent before and after SAC etching. Figure 74 shows the inline CD bias data after SAC etching based on 9 sites measurements. The average CD bias outside of the memory cells is only around 0.006 μm. However, the average CD bias inside the memory cells is slightly bigger than the regular inline measurement spot and is around 0.01 μm. Figure 75 shows the cross-section SEM pictures for SiN etching and standard contact etching. The standard contacts are located just above the gate area. It is very important to keep enough distance between the standard contact and SAC because the overlapped contacts cause the failure of the devices. The SAC etching step is very critical among the three etching steps because the higher selectivity of oxide over SiN is highly demanded. Therefore, most of the development work is focused on this particular step for the advanced technologies.

6.2.2 Development Work on the High-Density Plasma Tool

The SAC development work for 0.18 μm and below technologies starts on the high-density plasma tool first since the higher selectivity of oxide over SiN is obtained on this tool. The wafers were etched on the vendor's machine and the cross-section SEMs were done on site. The same model tool is purchased and installed in house after the



Center (memory cell)

Edge (memory cell)

Figure 73. Top-down CD SEM pictures before and after SAC etching
(Note: top – before SAC etching, bottom – after SAC etching.)

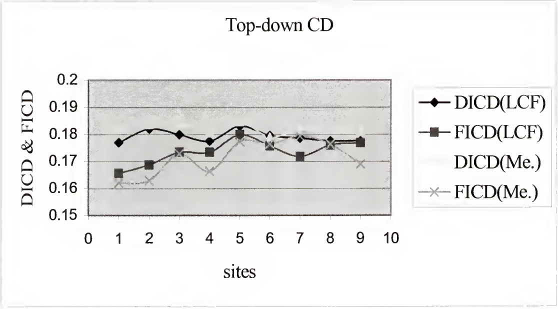
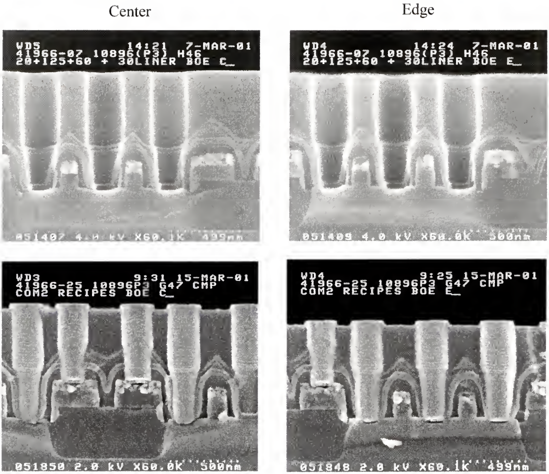


Figure 74. CD bias data after SAC etching inside and outside of memory cells



Center

Edge

Figure 75. Cross-section SEM pictures for SiN and standard contact etching processes (Note: top – SiN etching with BOE, bottom – standard contact etching with BOE.)

satisfied Demonstration (Demo) is finished. The process check on this new tool is different with the previous medium-density plasma tool. The gases CHF_3 and C_5F_8 are used for process check instead of C_4F_8 in the past. Gas calibration, wafer transportation, RF power calibration are completed during the installation. Three dummy wafers were etched before the process check in order to warm up the chamber after the installation. Table 4 shows the process check results on this new chamber. Both of CHF_3 and C_5F_8 recipes are used for etch rates check. There are 49 sites on every wafer to be measured on the Thermo-Wave machine. Etch rates and uniformities are very comparable with the specification data provided by the vendors. The selectivity of oxide over PR is also very comparable with the previous medium-density plasma etcher.

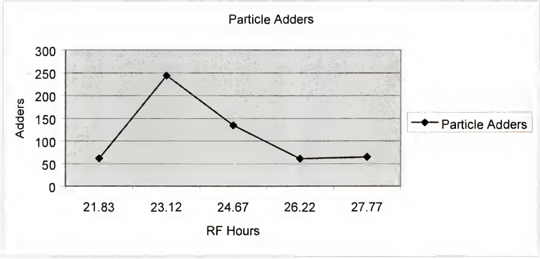
The Mini-marathon is set up based on the above results. It is designed for 100 wafers that are etched on the new chamber continually. The purpose of this experiment is to check the repeatability of the process, the stability of the performance of the new chamber. The responses are from wafer to wafer variation with one lot and from lot to lot variation. Additionally, RF hours are recorded to find the future cycle time. Table 5 shows the details of the Mini-marathon. The etch rate and particle adders are obtained from the blanket oxide wafers that are etched in the beginning, middle, and end of the marathon. The patterned 10 kÅ and 18 kÅ wafers are etched by using the baseline recipe as Table 5 indicated to collect the etching characterization data. The contact profile, CD bias, and selectivity of oxide over SiN are obtained on the cross-section SEM pictures of the 10 kÅ patterned wafers. The oxide etch depth is obtained from the cross-section SEM pictures of the 18 kÅ patterned wafers as mentioned previously. Figure 76 shows the particle adders and etch rates on the blanket wafers. The particle adders are dramatically

Table 4 - Initial process check results on the high-density plasma etcher

ER check for machine qualification		
a) CHF_3 recipe (dummy 3 wafers first)		
Wafer type	Data	Spec.
blanket Oxide	ER: 2355A/min	ER: 2200-2600A/min
	Uniformity: 2.16%	Uniformity: 8%
b) C_5F_8 recipe (dummy 3 wafers first)		
Wafer type	Data	Spec.
blanket Oxide	ER: 3488A/min	ER: 3400-3600A/min
	Uniformity: 1.18%	Uniformity: 5%
blanket PR	ER: 816A/min	ER: 800-1000A/min
	Uniformity: 0.25%	Uniformity: 10%
Selectivity of Ox/PR	4.3:1	

Table 5 - Experiment plan for the Mini-marathon

Mini-Marathon						
				Pre-	Post-	Delta
RF Hours						
21.50		slot 1	10k		PR Strip	
		slot 2	Ox	5005 @0.92%	2013@1.69%	2992
				adder: 8	adder: 70	62
		slot 3	10k		PR Strip	
		slot 4	18k			
		slot 5- slot22: PR dummy 18 wafers				
23.07		slot 23	Ox	5026@0.94%	1962@4.75%	3064
				adder: 15	adder:259	244
		slot 24	18k			
	lot 1	slot 25	10k		PR Strip	
	lot 2	slot 26- slot 50: PR dummy 25 wafers				
	end					
24.40		slot 51	10k			
		slot 52	Ox	5015@0.93%	2000@3.12%	3015
				adder: 68	adder: 203	135
		slot 53	18k			
	Lot 3	slot 54 - slot 75: PR summy 22 wafers				
26.13		slot 76	10k			
		slot 77	Ox	5022@0.93	1985@2.03%	3037
		slot 78	18k	adder: 7	adder: 68	61
		slot 79- slot 97: PR dummy 19 wafers				
		slot 98	Ox	4625@0.93	1965@2.04%	2660
				adder :6	adder: 71	65
		slot 99	18k			
27.46	lot 4	slot 100	10k			



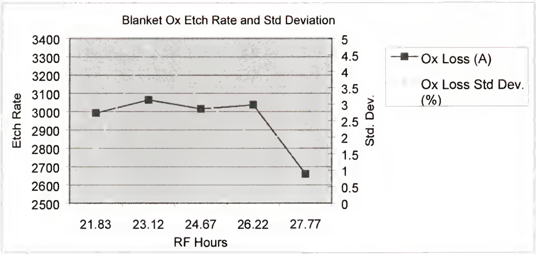


Figure 76. Etch rates and particle adders on the blanket wafers

increased and dropped immediately when RF hour is around 23 hours. The reason might be due to this particular wafer or the chamber needs more warm up time. The etch rate is decreased in the end of marathon. We think the possible reason might be due to the dirty chamber because we did a lot of testing experiments before this marathon. It is noticed that RF hours is around 21 hours in the beginning of the marathon. The correct procedure of the marathon should have the chamber cleaned before the marathon starts. However, we have to execute this marathon due to the tight schedule from the production engineers. Figure 77 shows the etch depth, SiN loss, and top CD vary with the wafer counts. The etch depth is gradually decreased as the wafer counts are increased. It indicates that the dirty chamber causes the slower etch rates. The average SiN loss is around 40 nm on the edge of the wafer across the whole marathon. However, the SiN loss is less than 40 nm in the middle of marathon on the center of the wafer. The quality of the specific wafer might cause the non-uniformity between center and edge at this particular point. The top CD is very consistent from the beginning of the marathon to the end of marathon.

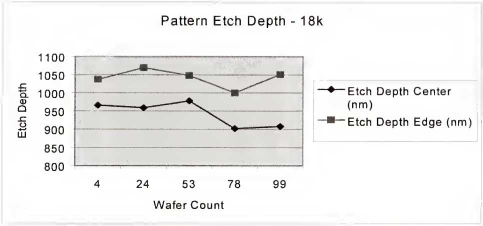
The process margin check is finished based on the results of Mini-marathon. The misalignment wafers on the Y direction are used intently to simulate the worst situation inline. Four etching parameters are investigated on the new chamber: O_2 gas flow, C_5F_8 gas flow, top RF power, and bottom RF power.

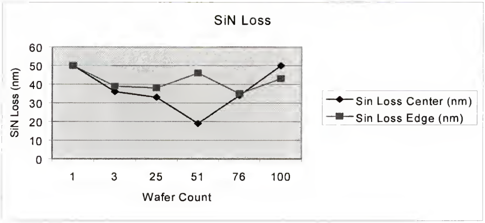
O_2 gas flow: 17 sccm – 19 sccm

C_5F_8 gas flow: 15 sccm – 17 sccm

top RF power: 800 W – 1000 W

bottom RF power: 1150 W – 1550 W





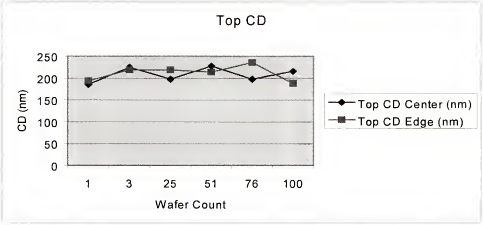
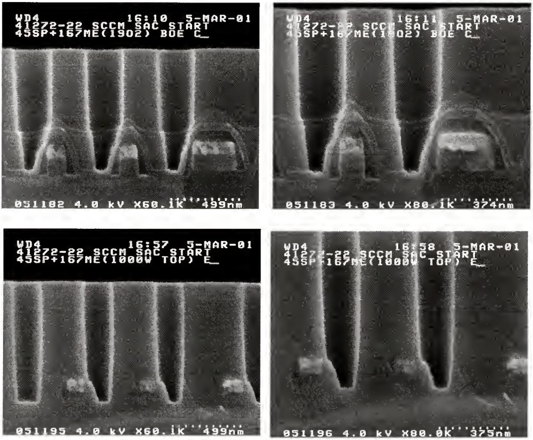


Figure 77. Etch depth, SiN loss, and Top CD vs wafer counts

Figure 78 shows the cross-section SEM pictures at the center point. The SiN loss is about 30 nm, the selectivity of oxide over SiN is around 15:1, and the selectivity of oxide over PR is about 9:1. Figure 79 shows the cross-section SEM pictures as O_2 gas flow varies. The center point still shows better uniformity and better selectivity of oxide over SiN. It is easy to have the etch stop either less O_2 gas flow or more O_2 gas flow based on the etch front of the profile. Therefore, we need to fix the O_2 gas flow to be 18 sccm. Figure 80 shows the cross-section SEM pictures as C_5F_8 gas flow varies. The similar trend is shown when we changed the C_5F_8 gas flow. The better controls on the uniformity and selectivity of oxide over SiN still are given on the baseline recipe. More C_5F_8 gas flow provides slight better selectivity of oxide over SiN, however, it is obvious to predict the etch stop in the end of the process based on the SEMs without 3 seconds BOE treatment. Figure 81 shows the effect of top RF power. The selectivity of oxide over SiN is comparable among three different top power settings. The center point is chosen again based on the etch front of the profile. Figure 82 shows the cross-section SEM pictures as bottom RF power changes. The uniformity is worse on either lower bottom RF power or higher bottom RF power. Certainly, the baseline point is chosen again as well. The baseline recipe on this high-density plasma etcher can provide 15:1 selectivity of oxide over SiN even on the misalignment wafers. It is much higher than the selectivity on the current medium-density plasma etcher that can only provide 10:1 selectivity of oxide over SiN.

Another type of high-density plasma etcher is also studied. This etch equipment is made from another vendor. The Zone testing wafers are provided by us and are etched on the vendor’s chamber. Figure 83 shows the Demo results from the vendor. The SiN loss


Center

Edge

Figure 78. Cross-section SEM pictures for baseline recipe
(Note: top – with BOE treatment, bottom – without BOE treatment.)

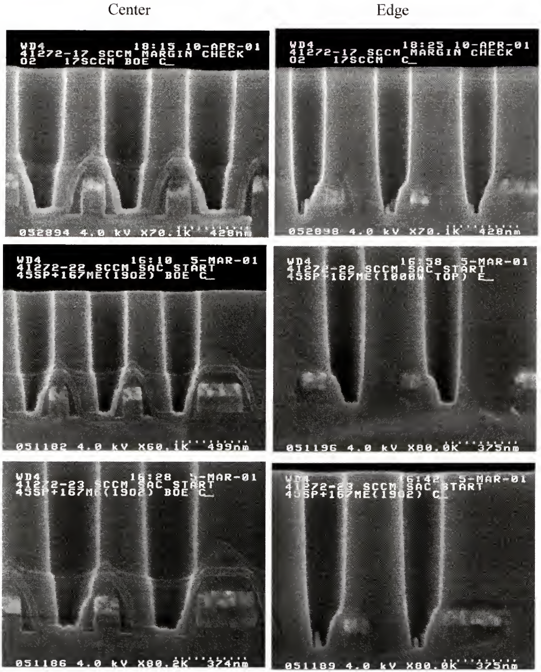


Figure 79. Cross-section SEM pictures as O_2 gas flow varies
(Note: top – 17 sccm O_2, middle – 18 sccm O_2, bottom – 19 sccm O_2, left – with BOE treatment, right – without BOE treatment.)

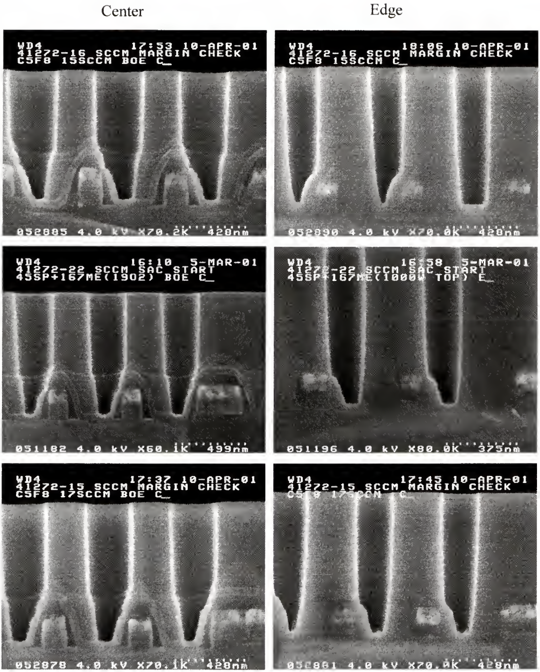


Figure 80. Cross-section SEM pictures as C_5F_8 gas flow varies
(Note: top – 15 sccm C_5F_8, middle – 16 sccm C_5F_8, bottom – 17 sccm C_5F_8, left – with BOE treatment, right – without BOE treatment.)

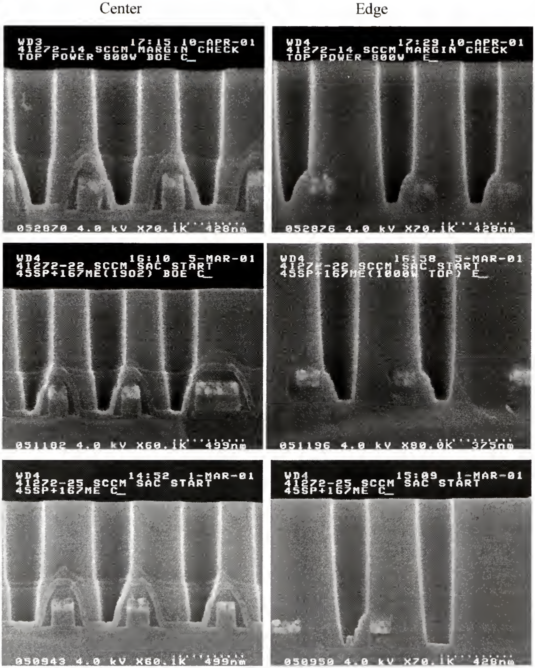


Figure 81. Cross-section SEM pictures as top RF power varies
(Note: top – 800 W, middle – 1000 W, bottom – 1200 W, left – with BOE treatment, right – without BOE treatment.)

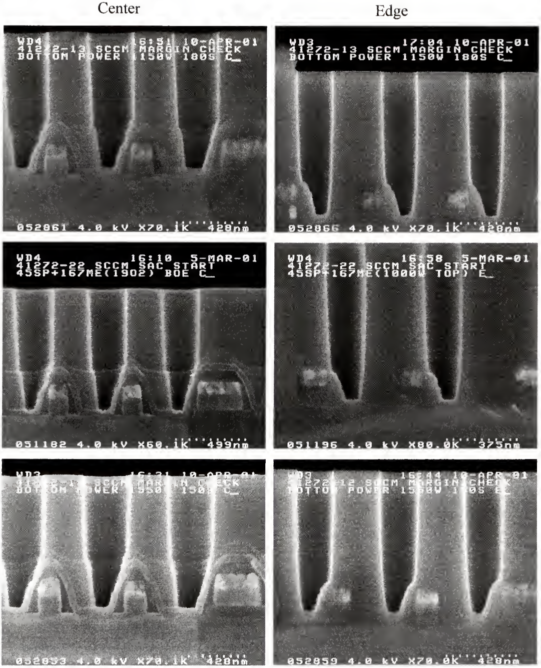

Center
Edge
WD4 16:51 10-APR-01
41272-13 SCCM MARGIN CHECK
BOTTOM POWER 1150W 180S C
052861 4.0 kV X70.1K 428nm
WD3 17:04 10-APR-01
41272-13 SCCM MARGIN CHECK
BOTTOM POWER 1150W 180S C
052866 4.0 kV X70.1K 428nm
WD4 16:10 5-MAR-01
41272-22 SCCM SAC START
455P+167ME(1902) BOE C
051182 4.0 kV X60.1K 499nm
WD4 16:58 5-MAR-01
41272-22 SCCM SAC START
455P+167ME(1000W TOP) E
051196 4.0 kV X80.0K 375nm
WD3 16:31 10-APR-01
BOTTOM POWER 1550W 150S C
052833 4.0 kV X70.1K 428nm
WD3 16:44 10-APR-01
41272-12 SCCM MARGIN CHECK
BOTTOM POWER 1550W 180S E
052859 4.0 kV X70.0K 428nm

Figure 82. Cross-section SEM pictures as bottom RF power varies (Note: top – 1150 W, middle – 1350 W, bottom – 1550 W, left – with BOE treatment, right – without BOE treatment.)

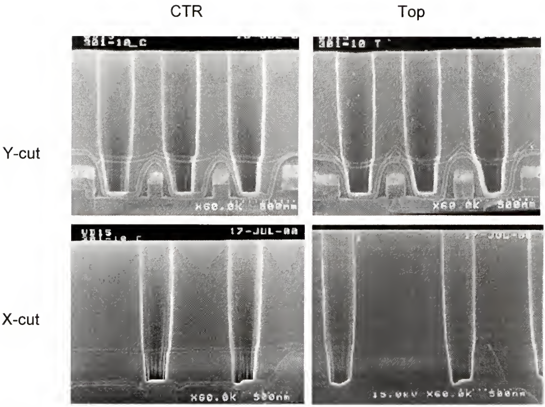


Figure 83. Cross-section SEM pictures on Demonstration (Demo) tool

is about 25 nm that is better than the first high-density plasma etcher. The novel gas — C_4F_6 is used in this process. However, this process cannot be duplicated on our own chamber that is purchased after the Demo is finished even though our tool is the same model with the Demo tool. The reason is that some hardware settings have to be changed on our tool for the Front End of Line (FEOL) applications. Either etch stop or SiN pouch through is obtained although the hardware settings are changed back to the original points. Finally, SAC etching development work has to be ended up on this particular tool due to its non-repeatability.

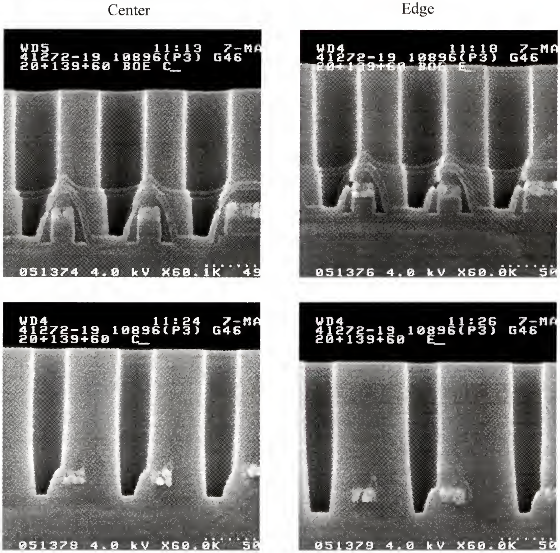
6.2.3 Development Work on the Medium-Density Plasma Tool

The SAC etching process development work has to be focused on the medium-density plasma tool because of the budget issue. The production lines cannot afford to buy more machines only for SAC application. Therefore, the decision is made to develop the SAC etching process on the current medium-density plasma tool although the process margin is very small and selectivity of oxide over SiN is extremely low. Two approaches are explored to increase the selectivity of oxide over SiN. One is to use the new gas — C_5F_8 in the main etching process based on the previous experience on the high-density plasma etcher, and another one is called "backup process" which means that the main etching time is reduced and the over etching time is increased to maintain the same etching target — 30% over-etch as before.

At first, the misalignment wafer is etched on the medium-density plasma tool by using the current POR recipe for 0.20 μm technology. It is a good reference data for us to develop the process for 0.18 μm and below technologies on the same tool. The process is a two-steps etching process and the gas C_4F_8 is used as pointed out previously. The etching target of main etching is about 10 kÅ and the etching target is around 3 to 4 kÅ for over etching. Figure 84 shows the cross-section SEM pictures for this POR process. The SiN layer is barely broken through on the center of the wafer and is completely broken through on the edge of the wafer. The etch rate of main etching is slightly faster than the etch rate of over etching. However, the selectivity of oxide over SiN is higher after the process is switched to over etching step. The selectivity of main etching is around 10:1 and it is around 20:1 during the over etching. The over etching step can also be called "soft-landing" process because it can provide less SiN gauging and higher selectivity. The gas CH_2F_2 is used in here to generate more polymers in order to protect the sidewall of the contact especially on the corner of the gate area. The integration requirement cannot be satisfied if the POR process is applied for the advanced technologies. The challenge is to increase the selectivity and keep the same over etching target without etch stop.

For C_5F_8 main etching process, the new gas — C_5F_8 replaces C_4F_8 due to the higher selectivity based on the experience on the high-density plasma etcher, and the same over etching process is still applied. The same etching target is reached during C_5F_8 main etching. Figure 85 shows the cross-section SEM pictures for this new process. The SiN loss is significantly improved on the corner of the gate area with 30% over etching. However, the contact resist is increased because more polymers are generated on the bottom of the contact and the contact hole size is shrunk.

For "backup process", gas C_4F_8 is still used on both of main etching and over etching steps. The only difference between this process and POR process is that the etching times of main etching and over etching are different. The new etching target in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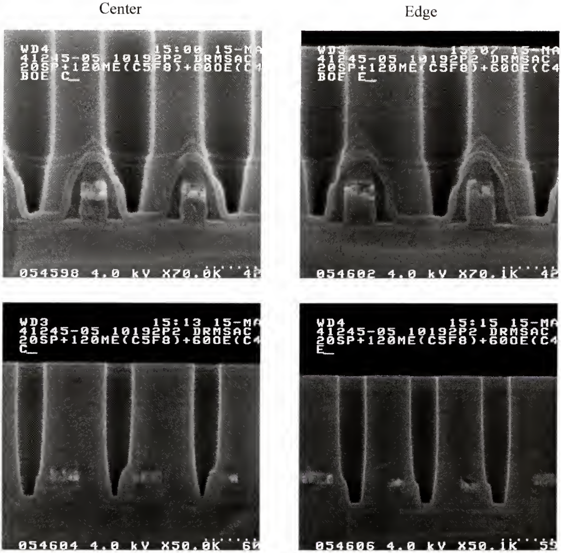
Edge

Figure 84. Cross-section SEM pictures by using Process of Record (POR) recipe (Note: top – with BOE treatment, bottom – without BOE treatment.)


Center

Edge

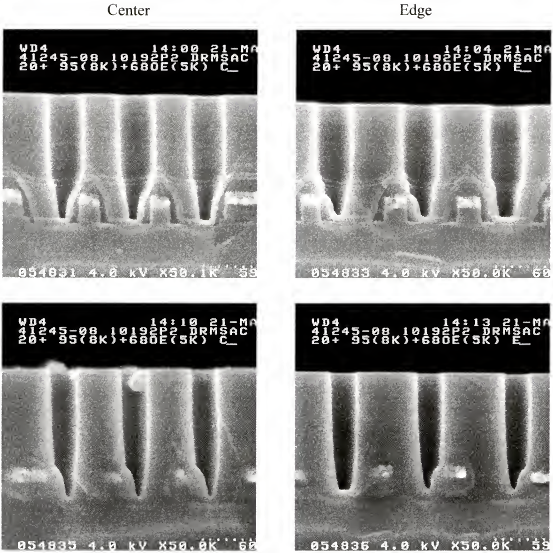
Figure 85. Cross-section SEM pictures by using new C_5F_8 process
(Note: top – with BOE treatment, bottom – without BOE treatment.)

main etching step is about 8 kÅ and is about 5 kÅ during over etching. The purpose of reducing the main etching target is to switch to the higher selectivity etching earlier before the corner of the gate area is hit. It means that the SiN loss margin on the corner of the gate area can be improved dramatically. Figure 86 shows the cross-section SEM pictures for this "backup process". The good SiN loss margin is observed from the SEM pictures and the etch depth can be reached to 13.4 kÅ.

Therefore, several split lots are etched on the same medium-density plasma tool by using POR recipe, C_5F_8 new process, and "backup process". One of the lots is intently misaligned printed to check the trend of the electrical results. The final electrical results tell us the "backup process" provides lower contact resistance and gate leakage for the aggressive design rules.

6.3 Final Recipe

The process margin check needs to be completed after the "backup process" is implemented inline for the development lots. The split is completed at the over etching step first. It means that the etching target in the main etching step has to be kept at 8 kÅ consistently and the etching target of over etching is changed from 4 kÅ to 6 kÅ. The electrical results on the first two split lots show the cell with 6 kÅ over etching target has much lower contact resistance and no gate leakage. Then the SAC process is changed to this process that has 8 kÅ main etching target and 6 kÅ over etching target. The new process margin check is completed based on this modified SAC process. The over etching target is changed from 5 kÅ to 7 kÅ and still keep the same main etching target — 8 kÅ. The center point process still shows the best electrical results consistently. The advanced process margin check work needs to be continued after the over etching target



Center

Edge

Figure 86. Cross-section SEM pictures by using "backup process"
(Note: top – with BOE treatment, bottom – without BOE treatment.)

is fixed at 6 kÅ. The lots are split among 7 kÅ, 8 kÅ, and 9 kÅ main etching targets and the over etching target is kept at 6 kÅ. The cell with 8 kÅ main etching target and 6 kÅ over etching target gives us the lowest contact resistance and gate leakage. Therefore, the final SAC recipe is fixed at 8 kÅ main etching target plus 6 kÅ over etching target. Another split lot is done to split 25 wafers between the development tool and the production tool as usual. The electrical results are very comparable in this split lot. This indicates the final SAC recipe is reproducible and it is qualified for being transferred to the manufacturing lines.

CHAPTER 7
SUMMARY AND FUTURE WORK

This dissertation investigated the challenges in the plasma etching processes for the dielectric materials in VLSI technology and showed the detailed development work on several dielectric etchers.

First of all, the fundamental concepts of plasma etching were introduced in the beginning of the dissertation. These important concepts included the different etching methods in the field of semiconductor fabrication, the physical mechanisms of plasma etching process, and different types of etch equipments for the different applications in the industry.

Secondly, the regular contact etching process for 0.18 μm below technology was developed and transferred to the manufacturing successfully on the medium-density plasma etcher. The aspect ratio was up to 5:1 for this advanced technology. The high selectivity of oxide over Si was obtained at 35:1, the CD bias was controlled tightly at 0.02 μm after contact dry clean, big process margin was achieved at 30% over etching. The satisfied electrical results were obtained on tens of lots. This process was transferred to the production lines completely.

Thirdly, the regular via etching process was introduced for 0.18 μm below technology. The key etching parameters were found to predict the process trend by analyzing the DOE results. The key parameters were: pressure, C_4F_8 gas flow, and O_2 gas flow. Therefore, the aggressive integration requirements were met successfully including the high selectivity of SiO_2 over TiN (up to 22:1), deeper over etching target (up to 50%

over etching), and the tight CD control after via clean (up to 0.02 μm). The special via etching process — tapered via etching was also studied extensively on the medium-density plasma etcher. There were two approaches for this particular application. One was called "Ex-situ process" and another one was called "In-situ process". The Ex-situ process contained main etching to shape the straight via profile, PR strip, and round corner step to round the corner of the top of the via. The advantage of this process was that the time for development work was much shorter. However, it asked longer cycle time and more over etching margin due to the thicker oxide layer. The In-situ process for 0.25 μm technology was delivered to the manufacturing lines successfully. It combined the TiN breakthrough step and round corner step together and shortened the cycle time. The yield has been improved significantly. The drawback of this process was that too much engineers' effort on the development work. The In-situ process for 0.18 μm below technology is still ongoing due to the aggressive design rules.

Finally, the SAC etching process was evaluated on several dielectric etching equipment. Much higher selectivity of oxide over SiN could be obtained on the high-density plasma etchers by using the novel gases – C_5F_8 or C_4F_6. However, the manufacturing engineers asked to develop the SAC etching process on the current medium-density plasma etchers because of the budget issues. One of approaches was to use the new gas – C_5F_8 in the main etching step to improve the selectivity of oxide over SiN. Another one was to reduce the main etching time and kept the same total etching target. The second one was called "backup process" and C_4F_8 was still used during main etching. The "backup process" showed higher selectivity of oxide over SiN, lower contact resistance, and no gate leakage for the tight design rules. The big advantage of the "backup process" was to save a lot of capitals for the company because no more new tools need to be purchased at this point.

Future work focuses on the improvement of selectivity of oxide over either TiN or SiN for even smaller feature size devices such as below 0.10 μm technology. Over etching margin and tight CD bias control are two of the challenges for the near future. Particularly, the In-situ process for the tapered via needs to be developed and transferred to the production lines soon because it will significantly increase throughput. The next generation etch equipment will be evaluated intensively in order to meet more aggressive design rules in VLSI technology.

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BIOGRAPHICAL SKETCH

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She joined the Bell Labs of Lucent Technologies, in Orlando, Florida in November 1998. She independently developed the contact and via etching processes in VLSI technology. All of the processes have been transferred to the production lines successfully and completely.

She joined TRW, in Redondo Beach, California in October 2001. She is currently developing the InP via etching process.

I certify that I have read this study and that in my opinion it conforms to acceptable standards of scholarly presentation and is fully adequate, in scope and quality, as a dissertation for the degree of Doctor of Philosophy.

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I certify that I have read this study and that in my opinion it conforms to acceptable standards of scholarly presentation and is fully adequate, in scope and quality, as a dissertation for the degree of Doctor of Philosophy.

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May 2002

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